**Project 5 - Memory Interface + Chip Spec**

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# 1. Introduction:

The designed System On Chip is able to communicate with a user via an Universal Asynchronous Receiver Transmitter (UART) interface to receive and transmit data. The SOC is also capable of interfacing to memory. The device that was used to verify the correctness of the SOC was the Digilent Nexys2 circuit board.

The SOC uses an external 8-bit microcontroller called PicoBlaze to receive and process data coming into and out of the SOC. The PicoBlaze is also able to process the status of the UART engine and inform the user whenever an overflow error or a parity error occurs within the UART communication. The UART engine achieves this by assigning status flags from its internal Receive engine. These flags are cleared every time that the PicoBlaze reads the status of the UART engine.

In order for the SOC to be able to accurately communicate with the user, they both need to set up an agreed upon communication scheme (number of data bits being sent, parity type, and number of stop bits). This is achieved by using the slide switches located on the Nexys2 board. Once the agreed upon communication scheme is established, the user then opens up a terminal window using the same communication scheme. This allows the SOC to communicate with the user and vice versa.

All that the user needs to do to initiate the SOC communication is to reset the system by pushing a reset button on the Nexys2 board. Upon reset, a banner is displayed and so is a command prompt (\*>). The user can then enter a character on the keyboard and its data is sent to the PicoBlaze. If the received character is a carriage return or a line feed character, then the PicoBlaze will have the UART Engine transmit a new line command and re-issue the prompt to the terminal window. If the character received is a pound sign (#), then the PicoBlaze will have the UART engine transmit the hometown of the developer (Porterville, CA) to the terminal window. If the received character is a backspace, then a destructive delete character is transmitted to the terminal which deletes that character from the terminal screen. For the SOC specifications, it is extremely important to make sure that the prompt does not get deleted when inputting a backspace or delete character on the keyboard. Any other valid ASCII character that the user enters on the keyboard will be echoed to the terminal.

Every character that the user enters into the keyboard is also written to the 8M x 16 Micron Memory located on the Nexys2 board starting at memory location 0x000. Each address location corresponds to 16 bits of data. Data can be written up to memory location 0x200 in the Micron Memory located on the Nexys2 board. Characters received after this limit is reached will begin to overwrite those characters previously saved in memory starting from the beginning at memory address 0x000.

Finally, in order to view the contents of the Micron Memory that have been written to, the user needs to send an asterisk (\*) to the PicoBlaze. This character causes the PicoBlaze to retrieve all of the memory data that has been written to (all of the characters that the user has pressed on their keyboard during the terminal session thus far) and display it on the terminal.

## 1.1.1 Requirements

1. This product displays the results of a working UART engine that is able to interface to Micron memory. Coming out of reset the controller should transmit a prompt to the screen. Whenever a byte is successfully received by the RX engine the controller will read the byte.

2. If the controller receives a back space (0x08) there should be a destructive delete (as long as there are characters to delete). Under no circumstances should the prompt be deleted.

3. When the controller receives a CR or LF it should respond with a newline and a prompt.

4. Every other printable ASCII character should be echoed.

5. Now, starting at location 0, each byte should also be written to the Micron memory. Remember that the Micron memory interface should be written and read 16-bits at a time.

6. When an asterisk ‘\*’ is received from the user, the data that has been written into the memory should be sent back to the user beginning with the first data byte received. Send a CR/LF first so that the dumped data begins at a new line.

7. After dumping the memory the controller should be ready to collect data again.

8. Every time you send a newline to the UART it should be followed by a prompt

9. When you delete a character on the terminal, it is not necessary to alter that character's stored value in memory.

10. This is an optional addition: When the controller receives a pound sign '#' this should cause the UART engine to respond with the home town of the designer.

# 2. Applicable Documents:

## 2.1.1 Applicable External Documents

[Digilent Nexys2 Board Reference Manual](https://www.digilentinc.com/Data/Products/NEXYS2/Nexys2_rm.pdf)

(https://www.digilentinc.com/Data/Products/NEXYS2/Nexys2\_rm.pdf)

[PicoBlaze 8-Bit Embedded Microcontroller User's Guide](http://www.xilinx.com/support/documentation/ip_documentation/ug129.pdf)

(http://www.xilinx.com/support/documentation/ip\_documentation/ug129.pdf)

[Spartan-6 Libraries Guide for HDL Designs](http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/spartan6_hdl.pdf)

(http://www.xilinx.com/support/documentation/sw\_manuals/xilinx11/spartan6\_hdl.pdf)

[Async/Page/Burst CellularRAM 1.5](http://datasheet.octopart.com/MT45W8MW16BGX-701IT-Micron-datasheet-138461.pdf)

(http://datasheet.octopart.com/MT45W8MW16BGX-701IT-Micron-datasheet-138461.pdf)

## 2.2.2 Applicable Internal Documents

There are no applicable internal documents for the SOC at this time.

# 3. Requirements:

## 3.1.1 Performance Requirements

The System On Chip (SOC) will be communicate using a Universal Asynchronous Receiver Transmitter (UART) interface. It will be able to communicate at the following baud rates: 300, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, and 460800.

## 3.1.2 Interface Requirements

The SOC will be using a Universal Asynchronous Receiver Transmitter (UART) interface. This interface will be used to asynchronously send data between the user and the SOC. The length of the data bits being sent and the format in which the data is sent is determined by the user at start-up using the slide switches on the Nexys2 board. The available formats for the SOC are 7N1, 7O1, 7E1, 8N1, 8O1, and 8E1. The first letter corresponds to the number of data bits that are going to be sent. The second letter corresponds to the parity of the communication type (no parity, odd parity, and even parity). The third letter corresponds to the number of stop bits that are going to be sent through the design to verify that all of the data bits have been received. The baud-rates supported by the SOC include 300, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, and 460800. Any baud-rates outside of these values have not been integrated into the design or they yield inconsistent results that impact the correctness of the data being sent through the UART interface (921600 Baud).

Technology Specific Instantiations should also be utilized in the design. For this project, the IOBUF and the OBUF TSI's have been implemented in the Memory Interface Block to help the data flow through the design.

## 3.1.3 Partitioning Requirements

After testing the design, I concluded that the baud rate of 921600 yielded inconsistent results in transmitting and receiving data using a UART communication scheme, so I decided to exclude this baud rate from the available baud rates that my SOC can communicate at.

## 3.1.4 Physical Requirements

This section should define any limitations placed on the design with respect to gate count, pin count, etc.

## 3.1.5 Power Requirements

A 3.3V power supply will drive the SOC.

## 3.1.6 Environmental Requirements

The SOC will be able to operate between 0**°** C – 70**°** C.

# 4. Top Level Design:

## 4.1.1 Top Level / Data Flow Description

The project consists of six different blocks. The first block in the Block Diagram is the Asynchronous In, Synchronous Out Synchronization Circuit. This makes it so that the reset button on the Nexys 2 Board (which is high-active) generates a low signal every time it is activated. This is because all of the reset logic in the system (excluding the external PicoBlaze microcontroller is low-active). The output of my AISO (rstsb) goes to all of the other blocks in the design. Because the PicoBlaze has a high-active reset, I needed to invert the rstsb output before I connected the rstsb signal to the PicoBlaze.

The second block in the design is the PicoBlaze. I use the PicoBlaze to process all of the data coming in from the Universal Asynchronous Receiver Transmitter interface terminal. I also use the PicoBlaze to determine what data is going to be transmitted to the terminal. The port\_id, write\_strobe, and read\_strobe outputs go into the third block, which is a decoder that I use to determine what data to write to the terminal and what data to read from the UART interface.

The fourth block consists of the transmit engine, where I format the data bits in the correct sequence and determine the parity, number of bits, and baud rate at which to transmit the data. I then shift load this data into a shift register and shift out the data bits individually until all of the bits have been transmitted to the terminal. The transmit engine also outputs a TxRdy flag to let the PicoBlaze know when it is ready to transmit another byte.

The fifth block consists of the receive engine. This block receives data from the terminal by determining the parity, number of bits, and baud rate at which the data is being received. The data bits are shifted into a shift register. Once all data bits have been shifted in, the receive engine then loads the received byte into a register and calculates the parity error. The receive engine also continually updates the overflow flag to make sure that an overflow does not occur (when the receive engine starts receiving another byte before it finishes receiving the previous byte). The receive engine outputs both the received byte of data and its status flags (Overflow, Parity Error, and RxRdy). The received byte of data is then sent over to the PicoBlaze so it can process it and figure out what to transmit to the terminal.

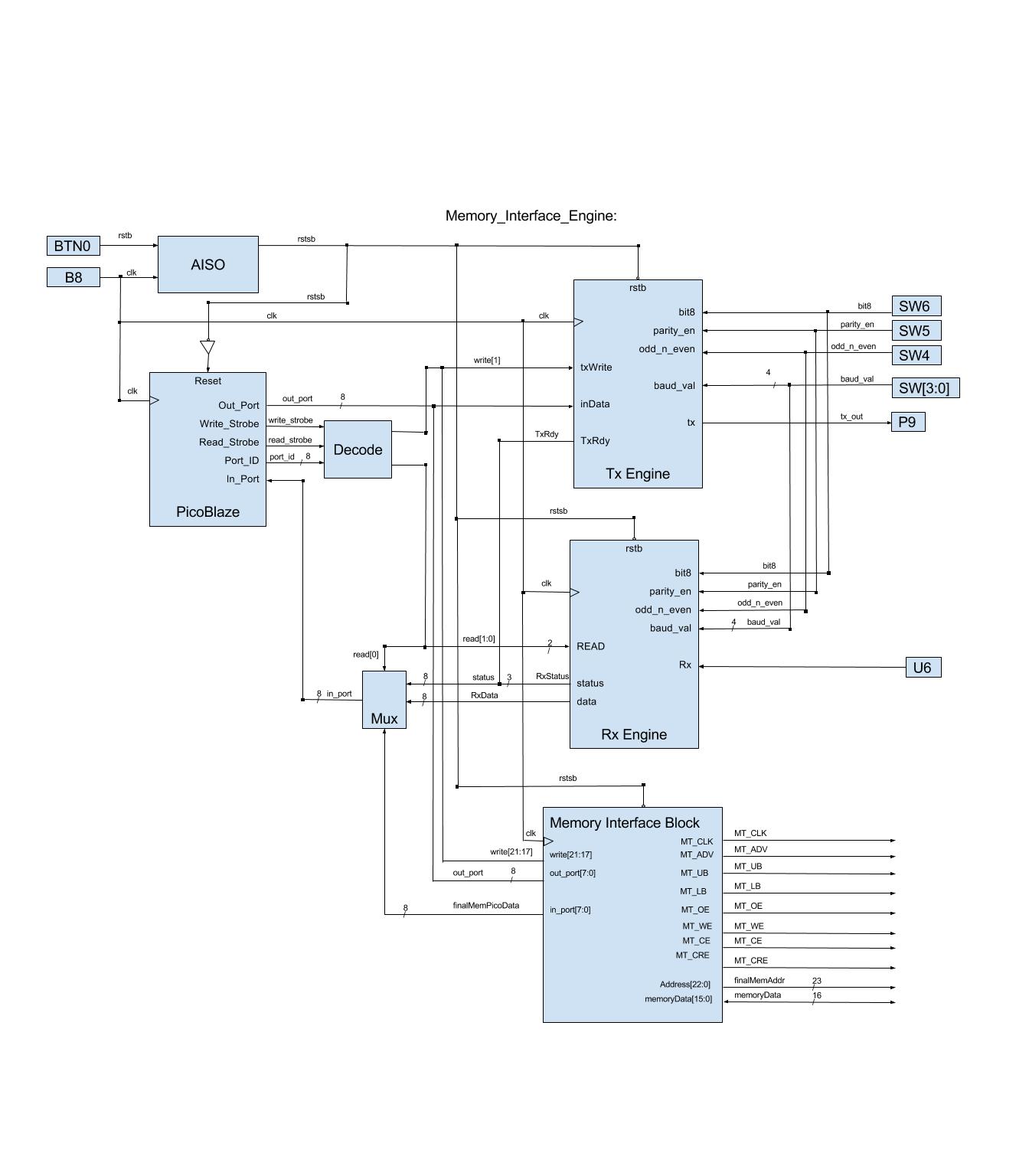
Both the receive engine status flags and the transmit engine status flags are concatenated together and they then go into the sixth block, which is a multiplexer. The multiplexer decides what 8 bits of data to send to the in\_port of the PicoBlaze based on whether read[0] is set high. If it is, then the in\_port of the PicoBlaze gets the status flags {2'b0, Overflow, ParityError, 2'b0, TxRdy, RxRdy}, otherwise it gets the received byte data from the receive engine.

The seventh block consists of the Memory Interface Block, where I have the logic to read and write from and to memory. This block relies on the data coming from the PicoBlaze and it also helps input specific data to the PicoBlaze as well. It internally creates the signals needed to perform read and write operations from and to memory. The memory interface status also goes into the multiplexor that the UART status flags and the receive engine data.

That sums up the main top-level design of my project.

I also connected a Seven-Segment Display in my design so that I can view the data being recieved by the PicoBlaze and see how many characters are displayed on the serial window line. For the sake of simplicity, however, I am not including this block in my top-level block diagram because it is trivial and does not contribute to the overall completion of the project.

## 4.1.2 Block Diagram



## 4.1.3 I/O

* (I) bit8 (1: 8 bits, 0: 7 bits)

Pin Assignment: N17 (SW 6)

* (I) parity\_en (1: parity enabled, 0: no parity)

Pin Assignment: L13 (SW5)

* (I) odd\_n\_even: (1: odd parity, 0: even parity)

Pin Assignment: L14 (SW 4)

* (I) baud\_val: (4 bits wide / combinations determine the baud rate at which the UART engine will run at)

Pin Assignment: K17 (SW 3), K18 (SW 2), H18 (SW 1), G18 (SW 0),

* (O) tx: Data bit being shifted out from Transmit Engine.

Pin Assignment: P9

* (I) Rx: Data bit being shifted into the Receive Engine.

Pin Assignment: U6

* (I) clk: Clock signal that drives the system

Pin Assignment: B8

* (I) rstb: Reset signal that is disbursed to the entire system.

Pin Assignment: B18

* (O) MT\_CLK : synchronizes memory to the system operating frequently during synchronous operations

Pin Assignment: H15

* (O) MT\_ADV : Indiactes that a valid address is present on the address inputs.

Pin Assignment: J4

* (O) MT\_UB : Upper Byte Enable DQ[15:8]

Pin Assignment: K4

* (O) MT\_LB : Lower Byte Enable DQ[7:0]

Pin Assignment: K5

* (O) MT\_OE: Outut Enable

Pin Assignment: T2

* (O) MT\_WE : Write Enable

Pin Assignment: N7

* (O) MT\_CE : Chip Enable

Pin Assignment: R6

* (O) MT\_CRE : Control Register Enable

Pin Assignment: P7

* (O) memWriteAddr [22:0] : Address inputs

Pin Assignment: K6 (memWriteAddr[22]), D1 (memWriteAddr[21]),

K2 (memWriteAddr[20]), D2 (memWriteAddr[19]), C1 (memWriteAddr[18]),

C2 (memWriteAddr[17]), E2 (memWriteAddr[16]), M5 (memWriteAddr[15]),

E1 (memWriteAddr[14]), F2 (memWriteAddr[13]), G4 (memWriteAddr[12]),

G5 (memWriteAddr[11]), G6 (memWriteAddr[10]), G3 (memWriteAddr[9]),

F1 (memWriteAddr[8]), H6 (memWriteAddr[7]), H3 (memWriteAddr[6]),

J5 (memWriteAddr[5]), H2 (memWriteAddr[4]), H1 (memWriteAddr[3]),

H4 (memWriteAddr[2]), J2 (memWriteAddr[1]), J1 (memWriteAddr[0])

* (O) a3 : annode 3 for seven segment display

Pin Assignment: F15

* (O) a2 : annode 2 for seven segment display

Pin Assignment: C18

* (O) a1 : annode 1 for seven segment display

Pin Assignment: H17

* (O) a0 : annode 0 for seven segment display

Pin Assignment: F17

* (O) a : a cathode for seven segment display

Pin Assignment: L18

* (O) b : b cathode for seven segment display

Pin Assignment: F18

* (O) c : c cathode for seven segment display

Pin Assignment: D17

* (O) d : d cathode for seven segment display

Pin Assignment: D16

* (O) e : e cathode for seven segment display

Pin Assignment: G14

* (O) f : f cathode for seven segment display

Pin Assignment: J17

* (O) g : g cathode for seven segment display

Pin Assignment: H14

* (I/O) memoryData[15:0]: memory data coming to and from the Micron Memory.

Pin Assignment:

T1 (memoryData[15]), R3 (memoryData[14]), N4 (memoryData[13]),

L2 (memoryData[12]), M6 (memoryData[11]), M3 (memoryData[10]),

L5 (memoryData[9]), L3 (memoryData[8]), R2 (memoryData[7]),

P2 (memoryData[6]), P1 (memoryData[5]), N5 (memoryData[4]),

M4 (memoryData[3]), L6 (memoryData[2]), L4 (memoryData[1]),

L1 (memoryData[0])

## 4.1.4 Register Map

PicoBlaze Registers used:

s0 - (tx\_data) : holds the 8-bit data to be transmitted by the UART Engine

s2 - (rx\_data) : holds the 8-bit data to be received by the UART Engine

s1 : holds the 8-bit status flag data of the UART Engine

s3 - (char\_counter) : holds the 8-bit counter data that keeps track of how many characters have been transmitted on the current line (for destructive delete command)

s6 - (mem\_addr\_0) : holds the register responsible for bits [7:0] of the memory address.

s7 - (mem\_addr\_1) : holds the register responsible for bits [15:8] of the memory address.

s8 - (mem\_addr\_2) : holds the register responsible for bits [23:16] of the memory address.

s9 - (mem\_addr\_read0) : holds the temporary data bits [7:0] of the memory address.

sA - (mem\_addr\_read1) : holds the temporary data bits [15:8] of the memory address.

sB - (mem\_addr\_read2) : holds the temporary data bits [23:16] of the memory address.

sC - (mem\_range\_selector) : variable that is set once the full memory has been reached (which starts displaying the entire memory locations now instead of comparing the mem\_addr\_read values to the current memory address.

## 4.1.5 Clocks

All blocks in this design use one clock that runs at a frequency of 50MHz. This means that the clock has a period of 20 nanoseconds (1/50MHz).

## 4.1.6 Resets

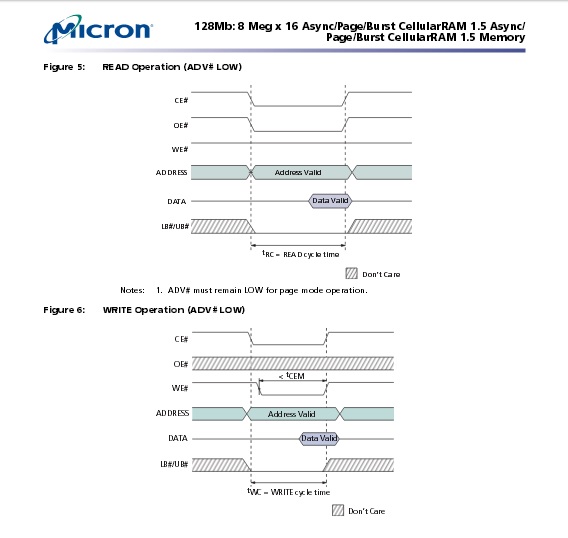
All original intellectual property (IP) developed for this design use an asynchronous, LOW active reset. The external PicoBlaze microcontroller in our design, on the other hand, uses an asynchronous HIGH active reset (meaning that we must feed an inverted reset value to the PicoBlaze).

## 4.1.7 Software

For the sake of readability, the software for this design is included at the end of the report.

## 4.1.8 Timing Information

In order to Read and Write from memory, the following timing diagrams for the CellularRam (Micron Memory) implemented in this design were taken into account:



\*Note: Picture taken from Spec-Sheet for the CellularRam.

# 5. Externally Developed Blocks:

## 5.1.1 PicoBlaze Description

\*NOTE: The following description, block diagram, I/O, and Register Maps were taken directly from the PicoBlaze Users Guide, which can be accessed [here](http://www.xilinx.com/support/documentation/ip_documentation/ug129.pdf).

The PicoBlaze™ microcontroller is a compact, capable, and cost-effective fully embedded 8-bit RISC microcontroller core optimized for the Xilinx FPGA families. The KCPSM3 version described in this user guide occupies just 96 FPGA slices in a Spartan®-3 Generation FPGA which is only 12.5% of an XC3S50 device and a miniscule 0.3% of an XC3S5000 device. In typical implementations, a single FPGA block RAM stores up to 1024 program instructions, which are automatically loaded during FPGA configuration. Even with such resource efficiency, the PicoBlaze microcontroller performs a respectable 44 to 100 million instructions per second (MIPS) depending on the target FPGA family and speed grade.

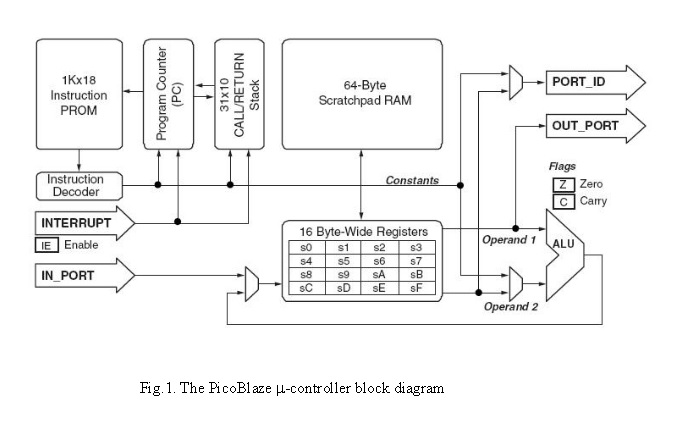
The KCPSM6 version of the PicoBlaze microcontroller is optimized for the Spartan-6, Virtex®-6, and 7 Series FPGAs and exploits the progress in technology to provide an even

higher degree of efficiency. The KCPSM6 microcontroller is a superset of KCPSM3 and is incredibly small occupying only 26 Slices.

The PicoBlaze microcontroller core is totally embedded within the target FPGA and requires no external resources. The PicoBlaze microcontroller is extremely flexible. The basic functionality is easily extended and enhanced by connecting additional FPGA logic to the microcontroller ’s input and output ports.

The PicoBlaze microcontroller provides abundant, flexible I/O at much lower cost than off-the-shelf controllers. Similarly, the PicoBlaze peripheral set can be customized to meet the specific features, function, and cost requirements of the target application. Because the PicoBlaze microcontroller is delivered as synthesizable VHDL source code, the core is future-proof and can be migrated to future FPGA architectures, effectively eliminating product obsolescence fears. Being integrated within the FPGA, the PicoBlaze microcontroller reduces board space, design cost, and inventory.The PicoBlaze FPC is supported by a suite of development tools including an assembler, a graphical integrated development environment (IDE), a graphical instruction set simulator, and VHDL source code and simulation models. Similarly, the PicoBlaze microcontroller is also supported in the Xilinx System Generator development environment.

## 5.1.2 PicoBlaze Block Diagram



## 5.1.3 PicoBlaze I/O

The Input/Output ports extend the PicoBlaze microcontroller’s capabilities and allow the microcontroller to connect to a custom peripheral set or to other FPGA logic. The PicoBlaze microcontroller supports up to 256 input ports and 256 output ports or a combination of input/output ports. The PORT\_ID output provides the port address. During an INPUT operation, the PicoBlaze microcontroller reads data from the IN\_PORT port to a specified register, sX. During an OUTPUT operation, the PicoBlaze microcontroller writes the contents of a specified register, sX, to the OUT\_PORT port.

Interface Signals:

* IN\_PORT[7:0] Input - Input Data Port: Present valid input data on this port during an INPUT instruction. The data is captured on the rising edge of CLK.
* INTERRUPT Input - Interrupt Input: If the INTERRUPT\_ENABLE flag is set by the application code, generate an INTERRUPT Event by asserting this input High for at least two CLK cycles. If the INTERRUPT\_ENABLE flag is cleared, this input is ignored.
* RESET Input - Reset Input: To reset the PicoBlaze microcontroller and to generate a RESET Event, assert this input High for at least one CLK cycle. A Reset Event is automatically generated immediately following FPGA configuration.
* CLK Input - Clock Input: The frequency may range from DC to the maximum operating frequency reported by the Xilinx ISE development software. All PicoBlaze synchronous elements are clocked from the rising clock edge. There are no clock duty-cycle requirements beyond the minimum pulse width requirements of the FPGA.
* OUT\_PORT[7:0] Output - Output Data Port: Output data appears on this port for two CLK cycles during an OUTPUT instruction. Capture output data within the FPGA at the rising CLK edge when WRITE\_STROBE is High.
* PORT\_ID[7:0] Output - Port Address: The I/O port address appears on this port for two CLK cycles during an INPUT or OUTPUT instruction.
* READ\_STROBE Output - Read Strobe: When asserted High, this signal indicates that input data on the IN\_PORT[7:0] port was captured to the specified data register during an INPUT instruction. This signal is asserted on the second CLK cycle of the two-cycle INPUT instruction. This signal is typically used to acknowledge read operations from FIFOs.
* WRITE\_STROBE Output - Write Strobe: When asserted High, this signal validates the output data on the OUT\_PORT[7:0] port during an OUTPUT instruction. This signal is asserted on the second CLK cycle of the two-cycle OUTPUT instruction. Capture output data within the FPGA on the rising CLK edge when WRITE\_STROBE is High.
* INTERRUPT\_ACK Output - Interrupt Acknowledge: When asserted High, this signal acknowledges that an INTERRUPT Event occurred. This signal is asserted during the second CLK cycle of the two-cycle INTERRUPT Event. This signal is optionally used to clear the source of the INTERRUPT input.

## 5.1.4 PicoBlaze Register Map

The PicoBlaze microcontroller includes 16 byte-wide general-purpose registers, designated as registers s0 through sF. For better program clarity, registers can be renamed using an assembler directive. All register operations are completely interchangeable; no registers are reserved for special tasks or have priority over any other register. There is no dedicated accumulator; each result is computed in a specified register.

The PicoBlaze microcontroller provides an internal general-purpose 64-byte scratchpad

RAM, directly or indirectly addressable from the register file using the STORE and FETCH instructions. The STORE instruction writes the contents of any of the 16 registers to any of the 64 RAM locations. The complementary FETCH instruction reads any of the 64 memory locations into any of the 16 registers. This allows a much greater number of variables to be held within the boundary of the processor and tends to reserve all of the I/O space for real inputs and output signals. The six-bit scratchpad RAM address is specified either directly (ss) with an immediate constant, or indirectly using the contents of any of the 16 registers (sY). Only the lower six bits of the address are used; the address should not exceed the 00 - 3F range of the available memory.

## 5.1.6 Micron Memory Description

\*NOTE: The following description, block diagram, I/O, and Register Maps were taken directly from the Micron Memory Specifications sheet, which can be accessed [here](http://datasheet.octopart.com/MT45W8MW16BGX-701IT-Micron-datasheet-138461.pdf).

Micron® CellularRAM™ is a high-speed, CMOS pseudo-static random access memory developed for low-power, portable applications. The MT45W8MW16BGX device has a 128Mb DRAM core, organized as 8 Meg x 16 bits. These devices include an industry-standard burst mode Flash interface that dramatically increases read/write bandwidth compared with other low-power SRAM or pseudo-SRAM offerings.

To operate seamlessly on a burst Flash bus, CellularRAM products incorporate a trans-parent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh.

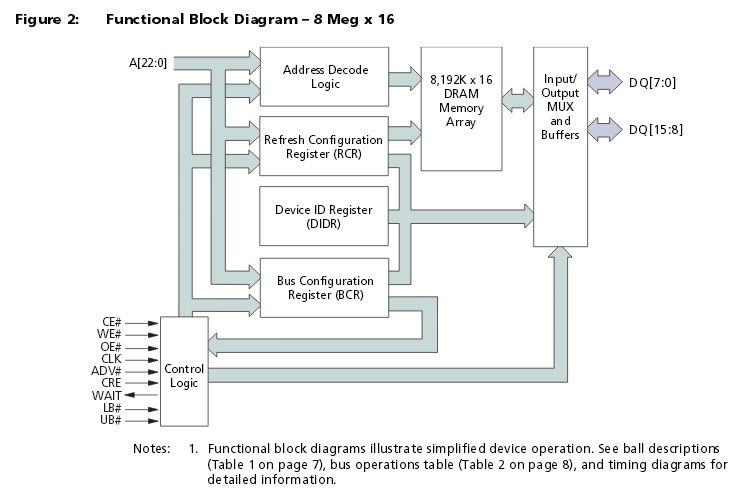
CellularRAM products include three mechanisms to minimize standby current. Partial-array refresh (PAR) enables the system to limit refresh to only that part of the DRAM array that contains essential data. Temperature-compensated refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature—the refresh rate decreases at lower temperatures to minimize current consumption during standby. Deep power-down (DPD) enables the system to halt the refresh operation altogether when no vital information is stored in

the device. The system-configurable refresh mechanisms are accessed through the RCR.

This CellularRAM device is compliant with the industry-standard CellularRAM 1.5

feature set established by the CellularRAM Workgroup. It includes support for both variable and fixed latency, with three output-device drive-strength settings, additional wrap options, and a device ID register (DIDR).

## 5.1.7 Micron Memory Block Diagram



## 5.1.8 Micron Memory I/O

Here are the corresponding Interface Signals for the MT45W8MW16BGX Micron Memory device:

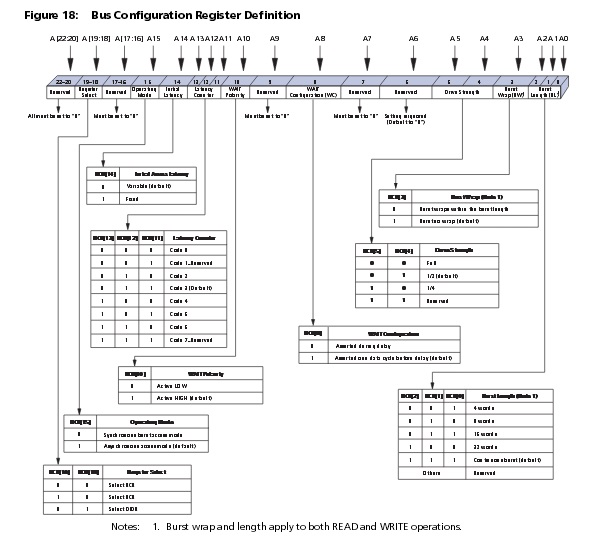
* A[22:0] Input - Address Inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR.
* CLK Input - Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK is static LOW during asynchronous access READ and WRITE operations and during PAGE READ ACCESS operations.
* ADV# Input - Address valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during asynchronous READ and WRITE operations. ADV# can be held LOW during asynchronous READ and WRITE operations.
* CRE Input - Control register enable: When CRE is HIGH, WRITE operations load the RCR or BCR, and READ operations access the RCR, BCR, or DIDR.
* CE# Input - Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is diisabled and goes into standby or deep power-down mode.
* OE# Input - Output Enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
* WE# Input - Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or the memory array.
* LB# Input - Lower Byte Enable: DQ[7:0]
* UB# Input - Upper Byte Enable: DQ[15:8]
* DQ[15:0] Input/Output - Data inputs/outputs.
* WAIT Output - Wait: Provides data-valid feedback during burst READ and WRITE operations. The signal is gated by CE#. WAIT is used to arbitrate collisions between refresh and READ/WRITE operations. WAIT is also asserted at the end of a row unless wrapping within the burst length. WAIT is asserted and should be ignored during asynchronous and page mode operations. WAIT is High-Z when CE# is HIGH.
* VCC Supply - Device Power Supply: (1.7 - 1.95V) Power supply for device core operation.
* VCCQ Supply - I/O Power Supply (1.7 - 3.6V) Power supply for input/output buffers.
* VSS Supply - VSS: must be connected to ground.
* VSSQ Supply - VSSQ: must be connected to ground.

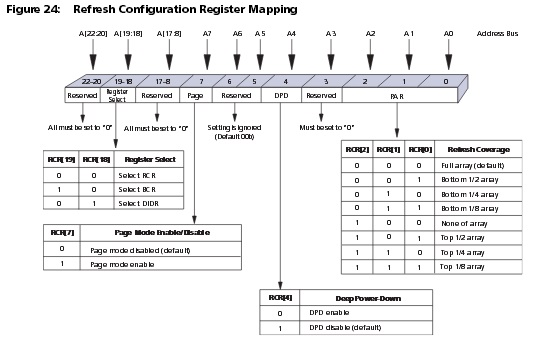
## 5.1.9 Micron Memory Register Map

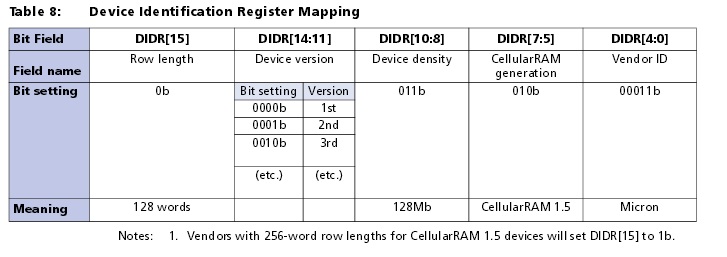
Two user-accessible configuration registers define the device operation. The BCR defines how the CellularRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The RCR is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up, and can be updated any time the devices are operating in a standby state.

A DIDR provides information on the device manufacturer, CellularRAM generation, and the specific device configuration. The DIDR is read-only.

The registers can be accessed using either a synchronous or an asynchronous operation when the control register enable (CRE) input is HIGH. (See Figures 12 through 15 on pages 18 through 21.) When CRE is LOW, a READ or WRITE operation will access the memory array. The configuration register values are written via addresses A[22:0]. In an asynchronous WRITE, the values are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are “Don’t Care.” The BCR is accessed when A[19:18] are 10b; the RCR is accessed when A[19:18] are 00b. The DIDR is read when A[19:18] are 01b. For reads, address inputs other than A[19:18] are “Don’t Care,” and register bits 15:0 are output on DQ[15:0]. Micron strongly recommends reading the memory array immediately after performing a configuration register READ or WRITE operation.



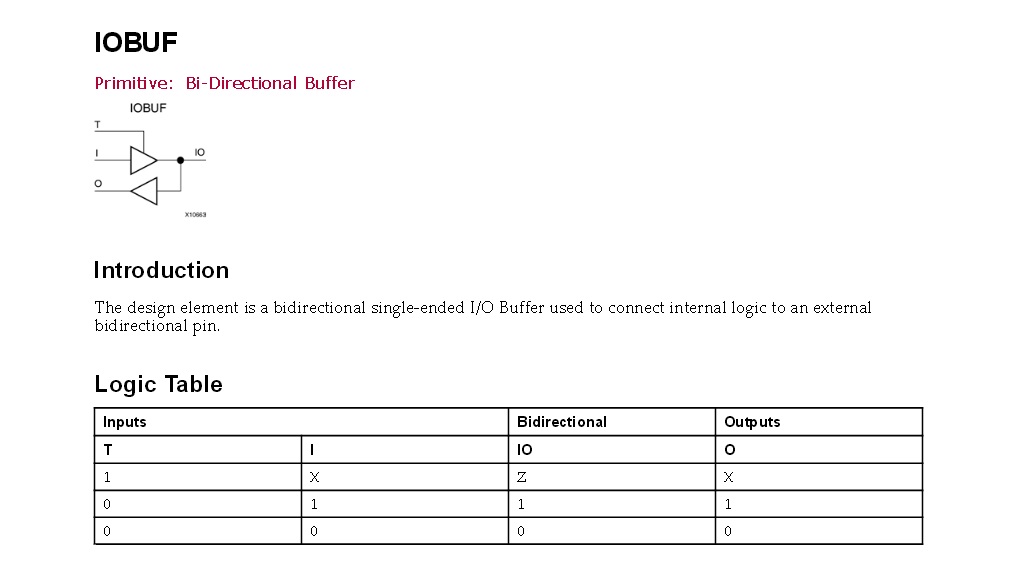




## 5.1.10 Technology Specific Instantiations Description

This SOC makes use of two different Technology Specific Instantiations within the design. I use an IOBUF to help me control the data going into and coming from the CellularRam memory connected to the Nexys2 board. I also use an OBUF to help buffer the memory address going into the CellularRam memory connected to the Nexys2 board. Please be advised that the following images are captured from the Spartan-6 Libraries Guide for HDL Design.

## 5.1.11 IOBUF TSI Block Diagram



## 5.1.12 IOBUF TSI I/O

## iobuff_inputs_outputs.jpg

## 5.1.13 IOBUF TSI Register Map

-N/A

## 5.1.14 OBUF TSI Block Diagram

## obuff.jpg

## 5.1.15 OBUF TSI I/0

## obuff_inputs_outputs.jpg

## 5.1.13 OBUF TSI Register Map

-N/A

# 6. Internally Developed Blocks: UART Engine

## 6.1.1 UART Engine Description

The SOC is using a Universal Asynchronous Receiver Transmitter (UART) interface to receive and transmit data. The UART Engine consists of both a Transmit Engine and a Receive Engine. The Transmit Engine is in charge of transmitting characters to the terminal and the Receive Engine is in charge of receiving the data that is coming from the terminal. The user sets up an agreed upon connection with the SOC and then opens up a terminal window. The UART Engine is connected to the 8-bit PicoBlaze Microcontroller, which is used to process and control the data going to and coming from the Transmit Engine. Upon reset, the PicoBlaze initiates the transmission of the banner by setting the appropriate character data and waiting until the Transmit engine is ready to transmit the next byte. It does this by reading in the status flags and monitoring the TxRdy output from the Transmit Engine. Upon reset, I have it so that my Transmit Engine is automatically ready to transmit a byte of data. Once the banner is transmitted, the PicoBlaze then transmits a prompt (\*>) to the terminal and waits for the user to enter a character onto the terminal. Once a character is entered, the Receive Engine then shifts in the character data one byte at a time. Once the byte is successfully shifted in, I then send this data over to the PicoBlaze so it can process the character received. It then determines what action to take based on what character the PicoBlaze received. If the character is a carriage return or a line feed character, then the PicoBlaze will transmit a new line command and re-issue the prompt to the terminal window. If the character is a carriage return or a line feed character, then the PicoBlaze will have the UART Engine transmit a new line command and re-issue the prompt to the terminal window. If the character is an asterisk (\*), then the PicoBlaze will have the UART Engine transmit the hometown of the developer (Porterville, CA) to the terminal window. Any other valid ASCII character that the user enters on the keyboard will be echoed to the terminal. The PicoBlaze is also able to process the status of the UART engine and informs the user whenever an overflow error or a parity error occurs within the UART communication. The status flags are cleared every time that the PicoBlaze reads the status of the UART engine.

I also added my Seven-Segment display to this lab so that I can display my character counter value on the upper 2 Seven-Segment displays and the data being received by the Receive Engine in the lower 2 Seven-Segment displays. This helped me out tremendously in verifying that I was receiving the proper character data.

## 6.1.2 UART Transmit Description

The Transmit Engine module contains all of the logic needed to transmit data via universal asynchronous receiver/transmitter (UART) communication. In order to create a stable UART connection, I needed to make sure that I could run my program at different baud rates and different data formats (7N1, 7O1, 7E1, 8N1, 8O1, 8E1). I also needed to make sure that both my program and the terminal software were running at the same baud-rate and data format.

In the Transmit Engine, I am shifting out the data in 12-bit data packets. I use a shift register to determine what data gets shifted out. I am able to load in the data that is going to be shifted out by delaying the write[1] strobe from the PicoBlaze by 1 clock cycle (this is because the data on the out\_port of the PicoBlaze is not available until the next clock cycle). If my write1Delay variable is set high, I then load my shift register with the out\_port data of the PicoBlaze, which I stored using a flop within my Transmit Engine. It is important to note that with UART communication, the least significant bit (lsb) of the data is sent out first and the most significant byte (msb) of the data is sent out last. I then update the remaining values in the shift register to make sure that I have accounted for the right parity, stop, and start bits. This is done using the bit8, parity\_en, and odd\_n\_even inputs and decoding their values so that I know what values to put in the b8, b7 bits of the shift register. Once all of the data in the shift register is accurate, I then start shifting out the bits 1 bit at a time. I fill the most significant bit of my shift register with a 1 (which is equivalent to filling up the register with a bunch of stop bits).

I keep track of when I am done shifting out all of the bits in my shift register by using a bit counter. In order to know when a bit is done being shifted out, I also needed to use a baud-rate counter. I first decoded the baud rate by reading in the data from my four baud\_rate switches. The next step was to determine what baud-rate I was running at based on those four switches. After determining the baud rate, I then needed to determine the amount of ticks I would need to count in order to achieve the specified baud-rate. I did this by using the formula baudCountNum = (1/baud rate) / (1/50MHz). This gave me the terminal count number that I needed to reach in order to run at the desired baud rate. I then assigned my baudCountNum variable to this terminal count value. Once that value was reached, I then knew that I had finished transmitting one bit via UART communication. Now the next step was to increment my Bit Counter. I repeated this process until my Bit Counter reached 11, meaning that I had finished transmitting all 12 bits of data in the data packet. For this project, I am always going to end up transmitting 12 bits of data per data packet. That is why my bit time counter limit is always 11 (0 to (12-1)). Once all 12 bits of data have been shifted out, I then set my Done variable to 1, which also sets my TxRdy variable to a 1. I then output this TxRdy variable, along with the other status variables to the PicoBlaze. These status variables are concatenated and represent the status register of the Transmit Engine. The TxRdy bit lets the PicoBlaze know that the Transmit Engine is ready to transmit another byte, at which point the PicoBlaze will output the next character being transmitted in the sequence to the Transmit Engine.

## 6.1.3 UART Receive Description

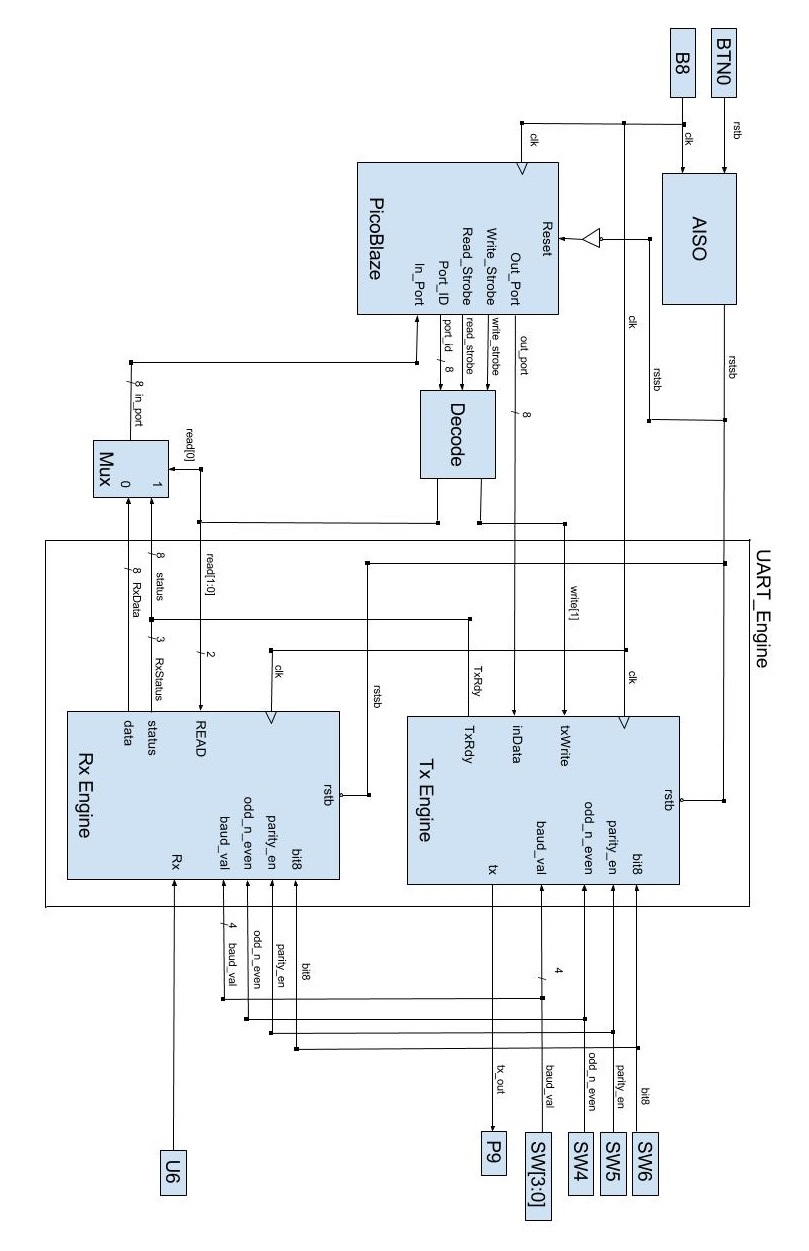
The Receive Engine module contains all of the logic needed to receive data via universal asynchronous receiver/transmitter (UART) communication. In order to create a stable UART connection, I needed to make sure that I could run my program at different baud rates and different data formats (7N1, 7O1, 7E1, 8N1, 8O1, 8E1). I also needed to make sure that both my program and the terminal software were running at the same baud-rate and data format.

My receive engine module contains all of the logic needed to receive information from a computer via universal asynchronous receiver/transmitter (UART) communication. In order to create a stable UART connection, I needed to make sure that I could run my program at different baud rates and different data formats (7N1, 7O1, 7E1, 8N1, 8O1, 8E1). For this program, I am shifting in the data from the receive engine 1-bit at a time. I use a shift register to store the receive engine data bits. Each data bit gets shifted in one bit at a time. For the receive engine we have a state diagram that consists of four different states: IDLE, S1, S2, and S3. The state machine starts off in the IDLE state at reset. In this state, it waits for a start bit (which is agreed to be a zero). We then move to the S1 state, where the state machine waits for half a bit-time. If the Rx input changes to a 1 during this half bit-time interval, I then move back to the IDLE state where we reset the bit-time interval and wait to receive a start bit value (0). If the Rx input stays the same (0) for the entirety of the half-bit time, this means that we actually received a start bit and I then move on to the next state, S2. I now know that we need to start collecting the data bits, so in S2, I wait for an entire bit time. After the bit time is achieved, I am know in the middle of the first data bit. I then move on to state S3, where I shift the data bit value into my shift register. I then check to see if all of the data bits have been shifted in to my shift register by checking the status of my bcu variable. This variable is set high for one clock cycle whenever all of the data bits have been received. If the bcu variable is set high, then I go back to the idle state where I wait until another bit is received. If the variable is not set high, then I go back to S2 and wait for another bit time so that I can shift in the next bit into the receive engine. Once all of the data bits have been shifted into the receive engine, I then send these data bits to the PicoBlaze so that it can process the received character and determine what to do with that data. I also send the status bits of the Rx Engine (OVERFLOW, PARITY\_ERR, and RxRdy) so that the PicoBlaze can inform the user if there were any errors in receiving the data. The OVERFLOW and PARITY\_ERR flags are cleared every time they are read from the Receive Engine.

The core buad rate and bit time counter logic are identical to that described in the transmit engine. There are a few minor differences, however. For one, I am using the DOIT variable generated in my state machine instead of the start bit generated in the Transmit Engine. In my baud rate counter logic, I also added in a multiplexer where I decide what value to load into the finalBaudCountNum variable. If my START variable is set high, then I know that I am waiting for the start bit of the received data. I then shift my baudCountNum to the right by 1. This divides the value by 2, which means that I am waiting for half of a bit time instead of the whole bit time. If the START variable is set low, then I know that I am waiting for the whole bit time and I keep my baudCountNum the same. Finally, I had to delay the done variable by one clock cycle in my design. Before I did this, my done bit was assigned when bcu was set high. This means that the done bit was automatically set high after the final bit time was achieved. This however, did not mean that the Receive Engine was finished yet because it still needed to load the final bit into the shift register. As a result, I was receiving overflow errors when trying to receive bytes in succession of each other because RxRdy was set high before the Rx Engine was finished receiving the data. In order to fix this, I delayed the done bit by putting it through a flop. This delayed the done bit for one clock cycle (which was enough time for the receive engine to load in the final data bit to the shift register). This fixed my overflow problem and allowed me to ensure that I was actually finished receiving the whole byte before I asserted the RxRdy bit.

The RxRdy bit is set high whenever it is ready to receive another byte. While the Receive Engine is receiving a byte, the RxRdy bit will be set low for the duration of the receive. When the Receive Engine is done receiving the byte, it then sends it to the PicoBlaze and then asserts the RxRdy flag so that it can notify the PicoBlaze that it is ready to receive another byte of data.

## 6.1.4 Block Diagram



## 6.1.5 I/O

* (I) bit8 (1: 8 bits, 0: 7 bits)

Pin Assignment: N17 (SW 6)

* (I) parity\_en (1: parity enabled, 0: no parity)

Pin Assignment: L13 (SW5)

* (I) odd\_n\_even: (1: odd parity, 0: even parity)

Pin Assignment: L14 (SW 4)

* (I) baud\_val: (4 bits wide / combinations determine the baud rate at which the UART engine will run at)

Pin Assignment: K17 (SW 3), K18 (SW 2), H18 (SW 1), G18 (SW 0),

* (I) txWrite: High active write enable
* (O) Txrdy: High active signal telling the PicoBlaze that it may write another byte
* (I) inData[7:0]: data from processor to be transmitted
* (O) tx: Data bit being shifted out from Transmit Engine.
* (I) READ[1:0]: High active READ enable
* (O) status[2:0]: Status bits of the Receive Engine (OVERFLOW, PARITY\_ERROR, RxRdy)
* (O) data[7:0]: data received from Receive Engine that should be passed to the PicoBlaze so that it can process the data.
* (I) Rx: Data bit being shifted into the Receive Engine.
* (I) clk: Clock signal that drives the system
* (I) rstb: Reset signal that is disbursed to the entire system.

## 6.1.6 State Machines

There is a state machine for the Rx Engine It is displayed on the next page.

There is also a state machine for the Debounce circuit in my debounce module. It is displayed after the Rx Engine State machine.

## 6.1.7 Register Map

PicoBlaze Registers used:

s0 - (tx\_data) : holds the 8-bit data to be transmitted by the UART Engine

s2 - (rx\_data) : holds the 8-bit data to be received by the UART Engine

s1 : holds the 8-bit status flag data of the UART Engine

s3 - (char\_counter) : holds the 8-bit counter data that keeps track of how many characters have been transmitted on the current line (for destructive delete command)

## 6.1.8 Transmit Engine Verification

For this Transmit Engine verification I created a test bench module for both my top\_level and my transmit\_engine files. For the top\_level test bench, all I did was initialize my inputs and set my baud-rate / data format to be 9600 / 8O1. I then ran the simulation and used the waveforms to verify that my Transmit Engine was storing/shifting the correct values out and that the PicoBlaze was outputting the character values at the appropriate times. The Transmit Engine test bench was a lot more involved than my top\_level test bench. In the Transmit Engine test bench, I made sure to test out a variety of data values and I also made sure that I was able to successfully run at all of the different baud-rates specified for my project. I also made sure that each data format (7N1, 7O1, 7E1, 8N1, 8O1m 8E1) worked correctly as well. I verified this by making sure that each 12-bit packet was transmitted in the correct order and by making sure that the appropriate values were being loaded into my shift register I also compared the desired shift register values to the actual shift register values and outputted the result to the console in order to help me debug my shift register and make sure that it was working properly. For a more detailed version of each test bench and its verification, refer to the header section of each test bench module within the source code. It is there that I go into further detail about how I verified the completeness of my design.

## 6.1.9 Receive Engine Verification

I verified that my Receive Engine was working correctly by using a simple test bench. In the Receive Engine test bench, I initialized my UART format to transfer at a baud rate of 460800 and have a format of 8O1. I then made sure that the receive engine correctly received the data of 0xAE. Since I extensively tested the Transmit Engine to make sure that I was able to successfully run at all of the different baud-rates and data formats (7N1, 7O1, 7E1, 8N1, 8O1m 8E1) for my project, I was convinced that the Receive Engine would yield the same results because the baud rate and format logic is almost identical between both engines. This is why I came to the conclusion that I did not need to test every possible baud-rate and data format combination for my Receive Engine. After I received the start bit from the receive data, I then waited for the bit time up to occur before I changed the Rx input value to the Receive Engine. This was so that I wasn't disturbing the Receive Engine while it was waiting for a bit time to begin collecting data. After a bit was shifted into the shift register, I then changed the Rx input in a way that would yield me receiving a byte of 0xAE. After all of the data bits were shifted into the shift register, I then loaded this data into a flop and sent the data to the PicoBlaze. As expected, the end result was that 0xAE was loaded into the flop and outputted to the PicoBlaze decoder (which selects what data is going to the In\_Port of the PicoBlaze) I also made sure that my Parity Error logic was correctly detecting a parity error by assigning the wrong parity to my byte of data. The 8O1 format should have an odd parity value of 0, but I gave the parity value a value of 1. As expected, The PARITY\_ERR status flag was set high and sent to the PicoBlaze decoder. I also made sure that all of my signals were changing correctly and that there were no surprises between the different states in my Receive Engine State Machine. This sums up what I did to verify the correctness of my Receive Engine. Note that I did not make a top level test bench for this project due to the sheer amount of transmits that I have to make for displaying the banner (it is a lot of characters!). Also, it is difficult to simulate the PicoBlaze receiving data because there is no terminal to display data through. This sums up how I verified the correctness of my Receive Engine.

# 7. Internally Developed Blocks: Memory Interface Block

## 7.1.1 Memory Interface Block Description

The memory interface block was pretty intuitive. There are three registers that I needed to retrive the whole memory address (because the PicoBlaze only outputs 8-bits of data at a time and the memory address is 23 bits wide). Each register is updated with the out\_port value of the PicoBlaze only when its appropriate write\_strobe data is set high. These three registers are then concatenated and go into an OBUF, where they are outputted and mapped to the address pin locations for the Micron memory. I also need two additional 8-bit registers to hold in the input data that is going to be written into memory (the memory data is 16-bits wide which is why I need two 8-bit registers). Like the address registers, each write data out register is only updated when its appropriate write\_strobe number is set high. Finally, I have two additional 8-bit registers (read data in registers) that hold the data values that are outputted by the specific memory address. These two registers are only updated once a Read operation from memory has successfully been completed. Both of the write data out registers are concatenated and go into the input of an IOBUF while the a 16-bit wire called rdDataIn goes to the output of the IOBUF. The read data in registers are updated with the correct values located inside of the rdDataIn 16-bit wire once a Read operation has finished executing in the Memory.

The write\_strobe and read\_strobe memory map is as follows

read\_strobe[0x00] ;read in status of transmit engine

read\_strobe[0x01] ;read in received data from receive engine

write\_strobe[0x11] ;output Write Address Register 0

write\_strobe[0x12] ;Write Address Register 1

write\_strobe[0x13] ;Write Address Register 2

write\_strobe[0x14] ;Write Data Out Register 0

write\_strobe[0x15] ;Write Data Out Register 1

read\_strobe[0x16] ;Read Data In Register 0

read\_strobe[0x17] ;Read Data In Register 0

write\_strobe[0x18] ;Perform Memory Read

write\_strobe[0x19] ;Perform Memory Write

read\_strobe[0x1A] ;Read in Memory Interface Status

Whenever the appropriate write\_strobe or read\_strobe was asserted, then the specific registers that relied on these signals were either updated or inputted to the PicoBlaze.

Apart from this logic, the Memory Interface Block needs a finite state machine to drive the signals that produce a Read or Write operation in memory. The signals being generated are the chip enable, output enable, and the write enable. For a write operation, the chip enable will be set low and so will the write enable. Since the write enable has precedence over the output enable, I do not care what the output enable is so I set it high for the entirety of the write operation. For the read operation, I set the write enable high and set the chip enable and output enable variables low for the entirety of the read operation. Both the read and write operations take approximately 85ns to finish, so I hold the appropriate values stable for 5 clock cycles (100ns) so that the data has enough time to finish. After those clock cycles are up, I then return the state machine to the idle state where it resets the signals to all be high and waits for the next operation to occur. Operations are only triggered when either write\_strobe[0x18] (perform memory read) or write\_strobe[0x19] (perform memory write) are asserted.

## 7.1.2 PicoBlaze Assembly

In order to get the PicoBlaze to successfully receive and transmit data via my UART Engine, I had to create my own assembly code where I process the received data and send the appropriate data to the Transmit Engine after the TxRdy bit from the status register was set high. Here is the assembly code that I wrote for this project:

;Memory Interface

;

;================================================================

; data constants

;================================================================

;selected ASCII codes

CONSTANT ASCII\_CR , 0D ; carriage return <CR>

CONSTANT ASCII\_LF , 0A ; line feed <LF>

CONSTANT ASCII\_Space , 20 ; Space

CONSTANT ASCII\_Asterisk , 2A ; \*(Asterisk) character

CONSTANT ASCII\_Greater\_Than, 3E ; >(Greater Than) character

CONSTANT ASCII\_bslash , 2F ; /(Backslash) character

CONSTANT ASCII\_colon , 3A ; :(colon) character

CONSTANT ASCII\_comma , 2C ; ,(comma) character

CONSTANT ASCII\_dash , 2D ; -(dash) character

CONSTANT ASCII\_exclamation , 21 ; !(exclamation point) character

CONSTANT ASCII\_backspace , 08 ; BS(backspace) character

CONSTANT ASCII\_delete , 7F ; DEL(descructive delete)

CONSTANT ASCII\_pound , 23 ;#(pound sign)

CONSTANT ASCII\_C\_U , 43 ; Uppercase C

CONSTANT ASCII\_E\_U , 45 ; Uppercase E

CONSTANT ASCII\_S\_U , 53 ; Uppercase S

CONSTANT ASCII\_4 , 34 ; number 4

CONSTANT ASCII\_6 , 36 ; number 6

CONSTANT ASCII\_0 , 30 ; number 0

CONSTANT ASCII\_V\_U , 56 ; Uppercase V

CONSTANT ASCII\_i , 69 ; Lowercase i

CONSTANT ASCII\_c , 63 ; Lowercase c

CONSTANT ASCII\_t , 74 ; Lowercase t

CONSTANT ASCII\_o , 6F ; Lowercase o

CONSTANT ASCII\_r , 72 ; Lowercase r

CONSTANT ASCII\_s , 73 ; Lowercase s

CONSTANT ASCII\_p , 70 ; Lowercase p

CONSTANT ASCII\_n , 6E ; Lowercase n

CONSTANT ASCII\_z , 7A ; Lowercase z

CONSTANT ASCII\_a , 61 ; Lowercase a

CONSTANT ASCII\_F\_U , 46 ; Uppercase F

CONSTANT ASCII\_u , 75 ; Lowercase u

CONSTANT ASCII\_l , 6C ; Lowercase l

CONSTANT ASCII\_U\_U , 55 ; Uppercase U

CONSTANT ASCII\_A\_U , 41 ; Uppercase A

CONSTANT ASCII\_R\_U , 52 ; Uppercase R

CONSTANT ASCII\_T\_U , 54 ; Uppercase T

CONSTANT ASCII\_D\_U , 44 ; Uppercase D

CONSTANT ASCII\_e , 65 ; Lowercase e

CONSTANT ASCII\_1 , 31 ; number 1

CONSTANT ASCII\_8 , 38 ; number 8

CONSTANT ASCII\_5 , 35 ; number 5

CONSTANT ASCII\_2 , 32 ; number 2

CONSTANT ASCII\_H\_U , 48 ; Uppercase H

CONSTANT ASCII\_m , 6D ; Lowercase m

CONSTANT ASCII\_w , 77 ; Lowercase w

CONSTANT ASCII\_P\_U , 50 ; Uppercase P

CONSTANT ASCII\_v , 76 ; Lowercase v

CONSTANT ASCII\_I\_U , 49 ; Uppercase I

CONSTANT ASCII\_Y\_U , 59 ; Uppercase Y

CONSTANT ASCII\_O\_U , 4F ; Uppercase O

CONSTANT ASCII\_L\_U , 4C ; Uppercase L

CONSTANT ASCII\_W\_U , 57 ; Uppercase W

CONSTANT ASCII\_M\_U , 4D ; Uppercase M

CONSTANT ASCII\_y, 79 ; Lowercase y

CONSTANT ASCII\_f , 66 ; Lowercase f

;================================================================

; port aliases

;================================================================

;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_input port definitions\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

CONSTANT rd\_flag\_port, 00 ;status of transmit engine

CONSTANT rx\_data\_port, 01 ;received data from receive engine

CONSTANT wr\_addr\_reg0, 11 ;Write Address Register 0

CONSTANT wr\_addr\_reg1, 12 ;Write Address Register 1

CONSTANT wr\_addr\_reg2, 13 ;Write Address Register 2

CONSTANT wr\_data\_reg0, 14 ;Write Data Out Register 0

CONSTANT wr\_data\_reg1, 15 ;Write Data Out Register 1

CONSTANT rd\_data\_reg0, 16 ;Read Data In Register 0

CONSTANT rd\_data\_reg1, 17 ;Read Data In Register 0

CONSTANT mem\_read, 18 ;Perform Memory Read

CONSTANT mem\_write, 19 ;Perform Memory Write

CONSTANT MIB\_Status, 1A ;Read in Memory Interface Status

NAMEREG s0, tx\_data ;data to be transmitted by uart

NAMEREG s2, rx\_data ;data to be received by uart

NAMEREG s3, char\_counter ;keeps track of how many characters have been

;transmitted on the current line (for destructive

;delete)

NAMEREG s6, mem\_addr\_0 ;memory address for Micron Memory

NAMEREG s7, mem\_addr\_1 ;memory address for Micron Memory

NAMEREG s8, mem\_addr\_2 ;memory address for Micron Memory

NAMEREG s9, mem\_addr\_read0 ;transmitting data received from memory

NAMEREG sA, mem\_addr\_read1 ;transmitting data received from memory

NAMEREG sB, mem\_addr\_read2 ;transmitting data received from memory

NAMEREG sC, mem\_range\_selector ;memory range selector

;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_output port definitions\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

CONSTANT uart\_tx\_port, 01 ;outputs to register 1 (Write\_Strobe[1])

;================================================================

; Main Program

;================================================================

main\_program:

load mem\_range\_selector, 00 ;zero out mem\_range\_selector

load char\_counter, 00 ;zero out the character counter

call zero\_out\_mem ;zero out memory locations 0x0 - 0x200

load mem\_addr\_0, 00 ;zero out memory address

load mem\_addr\_1, 00 ;zero out memory address

load mem\_addr\_2, 00 ;zero out memory address

load mem\_addr\_read0, 00 ;zero out counter for memory address

load mem\_addr\_read1, 00 ;zero out counter for memory address

load mem\_addr\_read2, 00 ;zero out counter for memory address

call display\_banner ;Display the banner at the beginning of the program

infinite\_loop:

call proc\_uart ;receive uart characters

JUMP infinite\_loop

;================================================================

; routine : check\_status\_flags

; function : check the status flags of the UART engine and inform the user of

; any errors that have occurred (parity, overflow)

; Input Register : s1 - read port flags

; Temp Register : s5 - check for parity/overflow error

; Output Register : tx\_data (s0) - data to be transmitted by uart

;================================================================

check\_status\_flags:

load s5, s1 ;copy status register value into s5

and s5, 20 ;isolate overflow bit

sub s5, 20 ;check to see if Overflow bit is set high

jump nz, check\_parity\_errror ;if it isn't, check the parity error flag

call display\_overflow\_error ;display overflow error

jump done\_error\_checking ;jump to the end of the error checking

check\_parity\_errror :

load s5, s1 ;copy status register value into s5

and s5, 10 ;isolate parity error bit

sub s5, 10 ;check to see if Parity Error bit is set high

jump nz, done\_error\_checking ;if it isn't, jump to the end of the error checking

call display\_pairty\_error ;display overflow error

done\_error\_checking:

return

;================================================================

; routine : tx\_one\_byte

; function : Wait until uart TxRdy bit is set, which signifies that the UART is

; ready to transmit another byte. Then transmit another byte to

; the UART.

; Input Register : s1 - read port flags

; Output Register : tx\_data (s0) - data to be transmitted by uart

;================================================================

tx\_one\_byte :

input s1, rd\_flag\_port ;read in status of the Transmit Engine

call check\_status\_flags ;check for overflow/parity errors

and s1, 02 ;isolate TxRdy bit

sub s1, 02 ; check to see if TxRdy bit is set high

jump nz, tx\_one\_byte ;if it isn't, keep on waiting until it is set high

output tx\_data, uart\_tx\_port ;If it is set high, then transmit byte to uart

compare tx\_data, ASCII\_delete ;check to see if data is a destructive delete

jump nz, increment\_counter

sub char\_counter, 01 ;decrement character counter

jump done\_updating\_counter

increment\_counter:

add char\_counter, 01 ;increment character counter

done\_updating\_counter:

output char\_counter, 05 ;output character counter value

return

;================================================================

; routine: proc\_uart

; function : receive UART input character and process it:

; CR - transmit a new line (CR/LF) and prompt

; LF - transmit a new line (CR/LF) and prompt

; \* - Dumps the memory that has been written to and displays it

; on the terminal window.

; # - Displays the designer's hometown (Porterville, CA)

; other - echo character

; every received character is also saved to Micron Memory

; Input Register : rx\_data(s2) - received data,

; s1 - read port flags,

; s4, MIB\_Status

; Output Register : tx\_data (s0) - data to be transmitted by uart

; mem\_addr\_read0 - address [7:0] used while dumping memory

; mem\_addr\_read1 - address [15:8] used while dumping memory

; mem\_addr\_read2 - address [23:16] used while dumping memory

; sD - used to output a value of 00 to controller

; mem\_addr\_0 - current address [7:0] of memory

; mem\_addr\_1 - current address [15:8] of memory

; mem\_addr\_2 - current address [23:16] of memory

; rx\_data

;================================================================

proc\_uart:

input rx\_data , rx\_data\_port ;receive data from terminal

receive\_byte:

input s1, rd\_flag\_port ;read in status of the Receive Engine

call check\_status\_flags ;check for overflow/parity errors

and s1, 01 ;isolate RxRdy bit

sub s1, 01 ; check to see if RxRdy bit is set high

jump nz, receive\_byte ;if it isn't, keep on waiting until it is set high

input rx\_data , rx\_data\_port ;store received data in register

compare rx\_data, ASCII\_pound ;see if pound sign was received

jump nz, compare\_cr ;if not, check for carriage return

call transmit\_hometown ;transmit hometown

call new\_prompt ;start a new line

jump uart\_receive\_byte\_done ;jump to store character in memory

compare\_cr:

compare rx\_data, ASCII\_CR ;see if carriage return was received

jump nz, compare\_lf ;if not, check for line feed

call new\_prompt ;trigger the newline prompt

jump save\_cr

compare\_lf:

compare rx\_data, ASCII\_LF ;see if line feed was received

jump nz, compare\_asterisk ;if not, check for asterisk

call new\_prompt ;trigger the newline prompt

jump save\_cr

compare\_asterisk:

compare rx\_data, ASCII\_Asterisk ;see if asterisk was received

jump nz, compare\_backspace ;if not, check for backspace

load tx\_data , ASCII\_CR

call tx\_one\_byte ; transmit CR (Carriage Return)

load tx\_data , ASCII\_LF

call tx\_one\_byte ; transmit LF (Line Feed)

load mem\_addr\_read0, 00 ;zero out counter for memory address read

load mem\_addr\_read1, 00 ;zero out counter for memory address read

load mem\_addr\_read2, 00 ;zero out counter for memory address read

begin\_mem\_rd:

output mem\_addr\_read0 , wr\_addr\_reg0 ;output [7:0] of memory address

output mem\_addr\_read1 , wr\_addr\_reg1 ;output[15:8] of memory address

output mem\_addr\_read2 , wr\_addr\_reg2 ;output [23:16] of memory address

compare mem\_range\_selector, 01 ;see up to what memory address to display to

jump nz, mem\_adr\_limit ;if not, check for backspace

compare mem\_addr\_read0, 02 ;see if values match

jump nz, get\_next\_mem\_loc ;if they don't get byte from memory

compare mem\_addr\_read1, 02 ;see if values match

jump nz, get\_next\_mem\_loc ;if they don't get byte from memory

call new\_prompt ;trigger the newline prompt

compare mem\_addr\_read2, 00 ;see if values match

jump z, uart\_receive\_byte\_done ;if they do, jump to end of process

jump get\_next\_mem\_loc ;

mem\_adr\_limit:

compare mem\_addr\_read0, mem\_addr\_0 ;see if values match

jump nz, get\_next\_mem\_loc ;if they don't get byte from memory

compare mem\_addr\_read1, mem\_addr\_1 ;see if values match

jump nz, get\_next\_mem\_loc ;if they don't get byte from memory

call new\_prompt ;trigger the newline prompt

compare mem\_addr\_read2, mem\_addr\_2 ;see if values match

load mem\_range\_selector, 01 ;zero out mem\_range\_selecto

jump z, uart\_receive\_byte\_done ;if they do, jump to end of process

get\_next\_mem\_loc:

load sD, 00 ; fill with zero value

output sD, mem\_read ;perform memory read

perform\_memory\_read:

input s4, MIB\_Status ;read in Memory Interface status

and s4, 01 ;isolate RDY bit

sub s4, 01 ; check to see if RDY bit is set high

jump nz, perform\_memory\_read ;if it isn't, keep on waiting until it is set high

input tx\_data , rd\_data\_reg0 ;Retrieve Read Data In Register 0

call tx\_one\_byte ;transmit data from memory

input tx\_data , rd\_data\_reg1 ;Retrieve Read Data In Register 1

call tx\_one\_byte ;transmit data from memory

add mem\_addr\_read0, 01 ;Increment memory address

addcy mem\_addr\_read1, 00 ;Incremetn memory address

addcy mem\_addr\_read2, 00 ;Incremetn memory address

jump begin\_mem\_rd ;get next memory location

compare\_backspace:

compare rx\_data, ASCII\_backspace ;see if backspace was received

jump nz, compare\_delete ;if not, check for destructive delete

compare char\_counter, 04 ;check to see if there are any bits to delete

jump z, done\_processing ;if there are no characters available to delete, do nothing

load rx\_data, ASCII\_delete ;load with a destructive delete if backspace pressed

jump transmit\_received\_char ;delete the character

compare\_delete:

compare rx\_data, ASCII\_delete ;see if delete was received

jump nz, echo\_character ;if not, echo character

compare char\_counter, 04 ;check to see if there are any bits to delete

jump z, done\_processing ;if there are no characters available to delete, do nothing

jump transmit\_received\_char ;transmit the destructive delete

echo\_character:

compare char\_counter, AA ;check to see if counter limit has been reached

jump nz, transmit\_received\_char ;if it isn't, transmit the character

call new\_prompt ;otherwise start a new line

transmit\_received\_char:

load tx\_data , rx\_data

call tx\_one\_byte ; echo received character

jump uart\_receive\_byte\_done;

save\_cr :

load rx\_data, ASCII\_CR

jump uart\_receive\_byte\_done ;

save\_lf :

load rx\_data, ASCII\_LF

uart\_receive\_byte\_done :

load sD, 00 ; fill with zero value

output mem\_addr\_0, wr\_addr\_reg0 ;output [7:0] of memory address

output mem\_addr\_1, wr\_addr\_reg1 ;output[15:8] of memory address

output mem\_addr\_2, wr\_addr\_reg2 ;output [23:16] of memory address

output rx\_data , wr\_data\_reg0 ;output [7:0] of memory address

output sD, wr\_data\_reg1 ;output [15:8] of memory address

output sD, mem\_write ;perform memory write

perform\_memory\_write:

input s4, MIB\_Status ;read in Memory Interface status

and s4, 01 ;isolate RDY bit

sub s4, 01 ; check to see if RDY bit is set high

jump nz, perform\_memory\_write ;if it isn't, keep on waiting until it is set high

compare mem\_addr\_0, 02 ;see if values match

jump nz, increment\_mem\_addr ;if they don't get byte from memory

compare mem\_addr\_1, 02 ;see if values match

jump nz, increment\_mem\_addr ;if they don't get byte from memory

compare mem\_addr\_2, 00 ;see if values match

jump nz, increment\_mem\_addr ;if they don't get byte from memory

load mem\_addr\_0, 00 ;roll over to beginning of memory

load mem\_addr\_1, 00 ;roll over to beginning of memory

load mem\_addr\_2, 00 ;roll over to beginning of memory

load mem\_range\_selector, 01 ;display all contents of memory from now on

jump done\_processing ;jump to end of command

increment\_mem\_addr :

add mem\_addr\_0, 01 ;Increment memory address

addcy mem\_addr\_1, 00 ;Incremetn memory address

addcy mem\_addr\_2, 00 ;Incremetn memory address

compare rx\_data, ASCII\_CR ;see if asterisk was received

jump z, save\_lf ;if not, increment address

done\_processing :

return

;================================================================

; routine: zero\_out\_mem

; function : writes a value of 0 to all of the memory locations:

;================================================================

zero\_out\_mem:

load mem\_addr\_0, 00 ;zero out memory address

load mem\_addr\_1, 00 ;zero out memory address

load mem\_addr\_2, 00 ;zero out memory address

next\_mem\_addr:

load sD, 00 ; fill with zero value

output mem\_addr\_0, wr\_addr\_reg0 ;output [7:0] of memory address

output mem\_addr\_1, wr\_addr\_reg1 ;output[15:8] of memory address

output mem\_addr\_2, wr\_addr\_reg2 ;output [23:16] of memory address

output sD , wr\_data\_reg0 ;output [7:0] of memory address

output sD, wr\_data\_reg1 ;output [15:8] of memory address

output sD, mem\_write ;perform memory write

fill\_memory\_with\_zero:

input s4, MIB\_Status ;read in Memory Interface status

and s4, 01 ;isolate RDY bit

sub s4, 01 ; check to see if RDY bit is set high

jump nz, fill\_memory\_with\_zero ;if it isn't, keep on waiting until it is set high

compare mem\_addr\_0, 02 ;see if values match

jump nz, increase\_mem\_addr ;if they don't get byte from memory

compare mem\_addr\_1, 02 ;see if values match

jump nz, increase\_mem\_addr ;if they don't get byte from memory

compare mem\_addr\_2, 00 ;see if values match

jump nz, increase\_mem\_addr ;if they don't get byte from memory

load mem\_addr\_0, 00 ;roll over to beginning of memory

load mem\_addr\_1, 00 ;roll over to beginning of memory

load mem\_addr\_2, 00 ;roll over to beginning of memory

jump done\_zeroing\_mem ;jump to end of command

increase\_mem\_addr :

add mem\_addr\_0, 01 ;Increment memory address

addcy mem\_addr\_1, 00 ;Incremetn memory address

addcy mem\_addr\_2, 00 ;Incremetn memory address

jump next\_mem\_addr ;if not, increment address

done\_zeroing\_mem :

return

;================================================================

; routine: display\_banner

; function : Transmits the beginning banner onto the terminal screen:

; \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

; \* CECS 460

; \* Victor Espinoza

; \* Full UART

; \* Due: 11/19/15

; \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;================================================================

display\_banner:

call transmit\_top\_of\_banner ;transmit asterisks

call transmit\_class ;transmit class name

call transmit\_student\_name ;transmit my name

call transmit\_project\_name ;transmit project name

call transmit\_due\_date ;transmit due date

call transmit\_top\_of\_banner ;transmit asterisks

load tx\_data , ASCII\_CR

call tx\_one\_byte ; transmit CR (Carriage Return)

load tx\_data , ASCII\_LF

call tx\_one\_byte ; transmit LF (Line Feed)

call new\_prompt ;transmit prompt

return

;================================================================

; routine: new\_prompt

; function : Transmits the new prompt (\*>) whenever a CR or LF chacacter

; are received or when the terminal issues a new line command.

;================================================================

new\_prompt:

load char\_counter, 00 ;zero out the character counter

load tx\_data , ASCII\_CR

call tx\_one\_byte ; transmit CR (Carriage Return)

load tx\_data , ASCII\_LF

call tx\_one\_byte ; transmit LF (Line Feed)

load tx\_data , ASCII\_Asterisk

call tx\_one\_byte ; transmit \* (Asterisk)

load tx\_data , ASCII\_Greater\_Than

call tx\_one\_byte ; transmit >(Greater Than)

return

;================================================================

; routine: transmit\_top\_of\_banner

; function : Transmits the top part of the banner (30 asterisks)

; \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

;================================================================

transmit\_top\_of\_banner:

load tx\_data , ASCII\_CR

call tx\_one\_byte ; transmit CR (Carriage Return)

load tx\_data , ASCII\_LF

call tx\_one\_byte ; transmit LF (Line Feed)

load sF, 1D ;

asterisk\_loop:

compare sF, 00 ; check to see if loop is done transmitting

jump z, done\_transmitting\_asterisks ; if it is, jump to end of loop

load tx\_data , ASCII\_Asterisk

call tx\_one\_byte ; transmit \* (Asterisk)

sub sF, 01 ; decrement loop counter

JUMP asterisk\_loop

done\_transmitting\_asterisks:

return

;================================================================

; routine: transmit\_class

; function : Transmits the class name (CECS 460)

;================================================================

transmit\_class:

load tx\_data , ASCII\_CR

call tx\_one\_byte ; transmit CR (Carriage Return)

load tx\_data , ASCII\_LF

call tx\_one\_byte ; transmit LF (Line Feed)

load tx\_data , ASCII\_Asterisk

call tx\_one\_byte ; transmit \* (Asterisk)

load tx\_data , ASCII\_Space

call tx\_one\_byte ; transmit space

load tx\_data , ASCII\_C\_U

call tx\_one\_byte ; transmit C

load tx\_data , ASCII\_E\_U

call tx\_one\_byte ; transmit E

load tx\_data , ASCII\_C\_U

call tx\_one\_byte ; transmit C

load tx\_data , ASCII\_S\_U

call tx\_one\_byte ; transmit S

load tx\_data , ASCII\_Space

call tx\_one\_byte ; transmit space

load tx\_data , ASCII\_4

call tx\_one\_byte ; transmit 4

load tx\_data , ASCII\_6

call tx\_one\_byte ; transmit 6

load tx\_data , ASCII\_0

call tx\_one\_byte ; transmit 0

return

;================================================================

; routine: transmit\_student\_name

; function : Transmits the student name (Victor Espinoza)

;================================================================

transmit\_student\_name:

load tx\_data , ASCII\_CR

call tx\_one\_byte ; transmit CR (Carriage Return)

load tx\_data , ASCII\_LF

call tx\_one\_byte ; transmit LF (Line Feed)

load tx\_data , ASCII\_Asterisk

call tx\_one\_byte ; transmit \* (Asterisk)

load tx\_data , ASCII\_Space

call tx\_one\_byte ; transmit space

load tx\_data , ASCII\_V\_U

call tx\_one\_byte ; transmit V

load tx\_data , ASCII\_i

call tx\_one\_byte ; transmit i

load tx\_data , ASCII\_c

call tx\_one\_byte ; transmit c

load tx\_data , ASCII\_t

call tx\_one\_byte ; transmit t

load tx\_data , ASCII\_o

call tx\_one\_byte ; transmit o

load tx\_data , ASCII\_r

call tx\_one\_byte ; transmit r

load tx\_data , ASCII\_Space

call tx\_one\_byte ; transmit space

load tx\_data , ASCII\_E\_U

call tx\_one\_byte ; transmit E

load tx\_data , ASCII\_s

call tx\_one\_byte ; transmit s

load tx\_data , ASCII\_p

call tx\_one\_byte ; transmit p

load tx\_data , ASCII\_i

call tx\_one\_byte ; transmit i

load tx\_data , ASCII\_n

call tx\_one\_byte ; transmit n

load tx\_data , ASCII\_o

call tx\_one\_byte ; transmit o

load tx\_data , ASCII\_z

call tx\_one\_byte ; transmit z

load tx\_data , ASCII\_a

call tx\_one\_byte ; transmit a

return

;================================================================

; routine: transmit\_project\_name

; function : Transmits the project name (Memory Interface)

;================================================================

transmit\_project\_name:

load tx\_data , ASCII\_CR

call tx\_one\_byte ; transmit CR (Carriage Return)

load tx\_data , ASCII\_LF

call tx\_one\_byte ; transmit LF (Line Feed)

load tx\_data , ASCII\_Asterisk

call tx\_one\_byte ; transmit \* (Asterisk)

load tx\_data , ASCII\_Space

call tx\_one\_byte ; transmit space

load tx\_data , ASCII\_M\_U

call tx\_one\_byte ; transmit M

load tx\_data , ASCII\_e

call tx\_one\_byte ; transmit e

load tx\_data , ASCII\_m

call tx\_one\_byte ; transmit m

load tx\_data , ASCII\_o

call tx\_one\_byte ; transmit o

load tx\_data , ASCII\_r

call tx\_one\_byte ; transmit r

load tx\_data , ASCII\_y

call tx\_one\_byte ; transmit y

load tx\_data , ASCII\_Space

call tx\_one\_byte ; transmit space

load tx\_data , ASCII\_I\_U

call tx\_one\_byte ; transmit I

load tx\_data , ASCII\_n

call tx\_one\_byte ; transmit n

load tx\_data , ASCII\_t

call tx\_one\_byte ; transmit t

load tx\_data , ASCII\_e

call tx\_one\_byte ; transmit e

load tx\_data , ASCII\_r

call tx\_one\_byte ; transmit r

load tx\_data , ASCII\_f

call tx\_one\_byte ; transmit f

load tx\_data , ASCII\_a

call tx\_one\_byte ; transmit a

load tx\_data , ASCII\_c

call tx\_one\_byte ; transmit c

load tx\_data , ASCII\_e

call tx\_one\_byte ; transmit e

return

;================================================================

; routine: transmit\_due\_date

; function : Transmits the project due date (Due: 12/10/15)

;================================================================

transmit\_due\_date:

load tx\_data , ASCII\_CR

call tx\_one\_byte ; transmit CR (Carriage Return)

load tx\_data , ASCII\_LF

call tx\_one\_byte ; transmit LF (Line Feed)

load tx\_data , ASCII\_Asterisk

call tx\_one\_byte ; transmit \* (Asterisk)

load tx\_data , ASCII\_Space

call tx\_one\_byte ; transmit space

load tx\_data , ASCII\_D\_U

call tx\_one\_byte ; transmit D

load tx\_data , ASCII\_u

call tx\_one\_byte ; transmit u

load tx\_data , ASCII\_e

call tx\_one\_byte ; transmit e

load tx\_data , ASCII\_colon

call tx\_one\_byte ; transmit : (Colon)

load tx\_data , ASCII\_Space

call tx\_one\_byte ; transmit space

load tx\_data , ASCII\_1

call tx\_one\_byte ; transmit 1

load tx\_data , ASCII\_2

call tx\_one\_byte ; transmit 2

load tx\_data , ASCII\_bslash

call tx\_one\_byte ; transmit / (Backslash)

load tx\_data , ASCII\_l

call tx\_one\_byte ; transmit l

load tx\_data , ASCII\_0

call tx\_one\_byte ; transmit 0

load tx\_data , ASCII\_bslash

call tx\_one\_byte ; transmit / (Backslash)

load tx\_data , ASCII\_l

call tx\_one\_byte ; transmit l

load tx\_data , ASCII\_5

call tx\_one\_byte ; transmit 5

return

;================================================================

; routine: transmit\_hometown

; function : Transmits the student's hometown (Hometown - Porterville, CA)

;================================================================

transmit\_hometown:

call new\_prompt ; transmit prompt

load tx\_data , ASCII\_Space

call tx\_one\_byte ; transmit space

load tx\_data , ASCII\_H\_U

call tx\_one\_byte ; transmit H

load tx\_data , ASCII\_o

call tx\_one\_byte ; transmit o

load tx\_data , ASCII\_m

call tx\_one\_byte ; transmit m

load tx\_data , ASCII\_e

call tx\_one\_byte ; transmit e

load tx\_data , ASCII\_t

call tx\_one\_byte ; transmit t

load tx\_data , ASCII\_o

call tx\_one\_byte ; transmit o

load tx\_data , ASCII\_w

call tx\_one\_byte ; transmit w

load tx\_data , ASCII\_n

call tx\_one\_byte ; transmit n

load tx\_data , ASCII\_Space

call tx\_one\_byte ; transmit space

load tx\_data , ASCII\_dash

call tx\_one\_byte ; transmit dash

load tx\_data , ASCII\_Space

call tx\_one\_byte ; transmit space

load tx\_data , ASCII\_P\_U

call tx\_one\_byte ; transmit P

load tx\_data , ASCII\_o

call tx\_one\_byte ; transmit o

load tx\_data , ASCII\_r

call tx\_one\_byte ; transmit r

load tx\_data , ASCII\_t

call tx\_one\_byte ; transmit t

load tx\_data , ASCII\_e

call tx\_one\_byte ; transmit e

load tx\_data , ASCII\_r

call tx\_one\_byte ; transmit r

load tx\_data , ASCII\_v

call tx\_one\_byte ; transmit v

load tx\_data , ASCII\_i

call tx\_one\_byte ; transmit i

load tx\_data , ASCII\_l

call tx\_one\_byte ; transmit l

load tx\_data , ASCII\_l

call tx\_one\_byte ; transmit l

load tx\_data , ASCII\_e

call tx\_one\_byte ; transmit e

load tx\_data , ASCII\_comma

call tx\_one\_byte ; transmit comma

load tx\_data , ASCII\_Space

call tx\_one\_byte ; transmit space

load tx\_data , ASCII\_C\_U

call tx\_one\_byte ; transmit C

load tx\_data , ASCII\_A\_U

call tx\_one\_byte ; transmit A

return

;================================================================

; routine: display\_pairty\_error

; function : Informs user of parity error (PARITY ERROR!)

;================================================================

display\_pairty\_error:

load tx\_data , ASCII\_P\_U

call tx\_one\_byte ; transmit P

load tx\_data , ASCII\_A\_U

call tx\_one\_byte ; transmit A

load tx\_data , ASCII\_R\_U

call tx\_one\_byte ; transmit R

load tx\_data , ASCII\_I\_U

call tx\_one\_byte ; transmit I

load tx\_data , ASCII\_T\_U

call tx\_one\_byte ; transmit T

load tx\_data , ASCII\_Y\_U

call tx\_one\_byte ; transmit Y

load tx\_data , ASCII\_Space

call tx\_one\_byte ; transmit space

load tx\_data , ASCII\_E\_U

call tx\_one\_byte ; transmit E

load tx\_data , ASCII\_R\_U

call tx\_one\_byte ; transmit R

load tx\_data , ASCII\_R\_U

call tx\_one\_byte ; transmit R

load tx\_data , ASCII\_O\_U

call tx\_one\_byte ; transmit O

load tx\_data , ASCII\_R\_U

call tx\_one\_byte ; transmit R

load tx\_data , ASCII\_exclamation

call tx\_one\_byte ; transmit exclamation

call new\_prompt ; transmit prompt

return

;================================================================

; routine: display\_overflow\_error

; function : Informs user of overflow error (OVERFLOW ERROR!)

;================================================================

display\_overflow\_error:

load tx\_data , ASCII\_O\_U

call tx\_one\_byte ; transmit O

load tx\_data , ASCII\_V\_U

call tx\_one\_byte ; transmit V

load tx\_data , ASCII\_E\_U

call tx\_one\_byte ; transmit E

load tx\_data , ASCII\_R\_U

call tx\_one\_byte ; transmit R

load tx\_data , ASCII\_F\_U

call tx\_one\_byte ; transmit F

load tx\_data , ASCII\_L\_U

call tx\_one\_byte ; transmit L

load tx\_data , ASCII\_O\_U

call tx\_one\_byte ; transmit O

load tx\_data , ASCII\_W\_U

call tx\_one\_byte ; transmit W

load tx\_data , ASCII\_Space

call tx\_one\_byte ; transmit space

load tx\_data , ASCII\_E\_U

call tx\_one\_byte ; transmit E

load tx\_data , ASCII\_R\_U

call tx\_one\_byte ; transmit R

load tx\_data , ASCII\_R\_U

call tx\_one\_byte ; transmit R

load tx\_data , ASCII\_O\_U

call tx\_one\_byte ; transmit O

load tx\_data , ASCII\_R\_U

call tx\_one\_byte ; transmit R

load tx\_data , ASCII\_exclamation

call tx\_one\_byte ; transmit exclamation

call new\_prompt ; transmit prompt

return

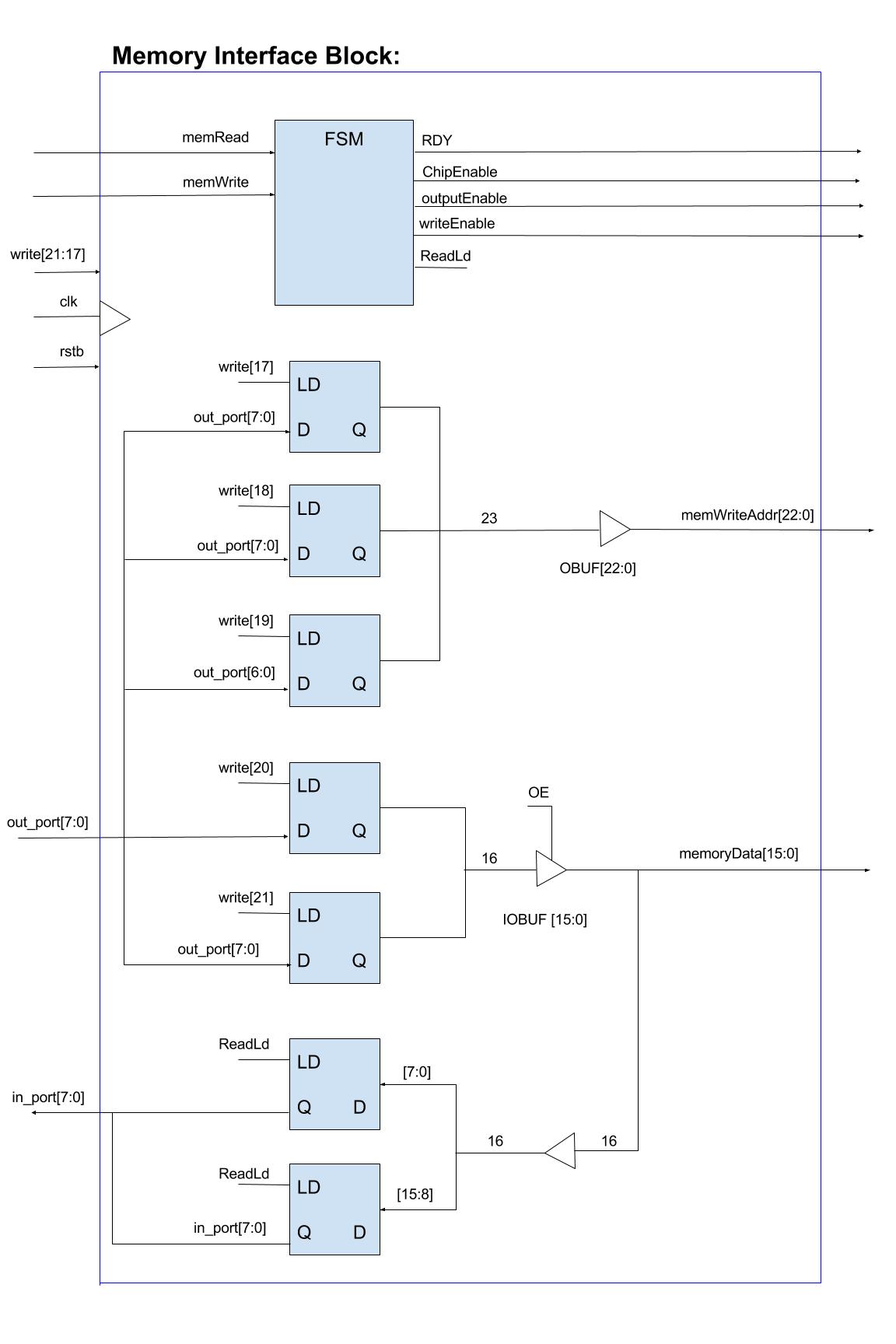
## 7.1.3 PicoBlaze Assembly Description

In my assembly code, I first define all of the constant values for the different ascii characters that I am going to be transmitting to the terminal. I then zero out the Micron memory locations 0x000 to 0x200 (which are the addresses that I decided to write to) and then transmit my banner which displays the project name, my name, and the due date for the project. I output all of these characters to the PicoBlaze's outport by repeatedly calling the tx\_one\_byte task. The tx\_one\_byte task is a fairly simple task that outputs the appropriate register value for the ASCII character to the PicoBlaze's output. Before I output the value, however, I have to make sure that the TxRdy bit is set high within the Transmit Engine, which signifies that the engine is ready to transmit the next byte. I achieve this by sending the status register of the Transmit Engine (which has the TxRdy bit as the second bit in the register) to the in\_port of the PicoBlaze. I use the input s1, rd\_flag\_port instruction to store the value of the status register into the internal PicoBlaze register s1. I then call another task called check\_status\_flags which checks the OVERFLOW and PARITY\_ERR flags set in the Receive Engine and transmits the appropriate message to the terminal if these flags are set high (OVERFLOW ERROR and PARITY ERROR, respectively). After returning from the check\_status\_flags routine, I then subtract 02 from the s1 value in order to check to see if the TxRdy bit is set high. If the TxRdy bit is not set high, that means that the Transmit Engine is not ready to transmit the current data yet, so I keep on looping back to the beginning of my tx\_one\_byte task, where I continually read in the status register values and wait until the TxRdy bit is set high. When TxRdy is high, I then output the appropriate character value to the PicoBlaze's out\_port using the Output instruction. I output the character value to the port\_id 01 because I want to use the write[1] write\_strobe for my transmitting signal.

Once I am done printing the banner, I then transmit my prompt(\*>) and wait for the user to send a character to the Receive Engine. I monitor this by constantly reading in the status flags and seeing when RxRdy is set high (which indicates that the Receive Engine has finished receiving a byte of data and is ready to receive another byte. I then compare this received data to my ASCII line feed, carriage return, asterisk, pound sign, and backspace / delete characters. If the received character happens to be one of these characters, then I perform the associated action that corresponds to that character (go to the next line and re-display the prompt, dump the saved memory data to the terminal, display my home town, and delete the previously transmitted character (if one is available). Otherwise I just echo the received character to the terminal window. I have a counter value that I increment every time a new character is transmitted onto the terminal screen and I decrement this counter whenever I delete a character. I have it so that the terminal window can store up to 170 (0xAA) characters on a line. If the user tries to enter a character that surpasses this limit, then I then issue a new line and prompt and then transmit the character as the first character that shows up after the new prompt on the next line.

Every time that the PicoBlaze receives a character, it automatically saves that character to memory as well. This is done by sending out the appropriate address to the memory interface block (MIB) and sending in the received character data. I monitor the MIB status flags while I am writing to memory to make sure that I am able to completely finish writing to memory before I proceed to the next part of my code. In this part, I basically just increment the address to the next position in memory and wait for the next character to be received. When an asterisk is pressed, I then display the contents of every value that has been stored to memory. For the purpose of this lab, I only wrote up to memory location 0x200. This was because I did not find it practical to have to write to a higher memory location (I already knew that the register increments worked in the design). In order to achieve this I have temporary registers that I use to hold the memory address starting at 0x000. I then compare it to the current memory address (stored in other registers) and if it does not match then I retrieve the contents stored at that memory location and transmit them to the UART Transmit Engine. That is the gist of how my Assembly code works. For a more detailed discussion refer to the comments in the actual assembly code itself.

## 7.1.4 Block Diagram



## 7.1.5 I/O

* (I) clk: Clock signal that drives the system

Pin Assignment: B8

* (I) rstb: Reset signal that is disbursed to the entire system.

Pin Assignment: B18

* (O) MT\_OE: Outut Enable

Pin Assignment: T2

* (O) MT\_WE : Write Enable

Pin Assignment: N7

* (O) MT\_CE : Chip Enable

Pin Assignment: R6

* (O) memWriteAddr [22:0] : Address inputs

Pin Assignment: K6 (memWriteAddr[22]), D1 (memWriteAddr[21]),

K2 (memWriteAddr[20]), D2 (memWriteAddr[19]), C1 (memWriteAddr[18]),

C2 (memWriteAddr[17]), E2 (memWriteAddr[16]), M5 (memWriteAddr[15]),

E1 (memWriteAddr[14]), F2 (memWriteAddr[13]), G4 (memWriteAddr[12]),

G5 (memWriteAddr[11]), G6 (memWriteAddr[10]), G3 (memWriteAddr[9]),

F1 (memWriteAddr[8]), H6 (memWriteAddr[7]), H3 (memWriteAddr[6]),

J5 (memWriteAddr[5]), H2 (memWriteAddr[4]), H1 (memWriteAddr[3]),

H4 (memWriteAddr[2]), J2 (memWriteAddr[1]), J1 (memWriteAddr[0])

* (I/O) memoryData[15:0]: memory data coming to and from the Micron Memory.

Pin Assignment:

T1 (memoryData[15]), R3 (memoryData[14]), N4 (memoryData[13]),

L2 (memoryData[12]), M6 (memoryData[11]), M3 (memoryData[10]),

L5 (memoryData[9]), L3 (memoryData[8]), R2 (memoryData[7]),

P2 (memoryData[6]), P1 (memoryData[5]), N5 (memoryData[4]),

M4 (memoryData[3]), L6 (memoryData[2]), L4 (memoryData[1]),

L1 (memoryData[0])

## 7.1.6 Register Map

PicoBlaze Registers used:

s0 - (tx\_data) : holds the 8-bit data to be transmitted by the UART Engine

s2 - (rx\_data) : holds the 8-bit data to be received by the UART Engine

s1 : holds the 8-bit status flag data of the UART Engine

s3 - (char\_counter) : holds the 8-bit counter data that keeps track of how many characters have been transmitted on the current line (for destructive delete command)

s6 - (mem\_addr\_0) : holds the register responsible for bits [7:0] of the memory address.

s7 - (mem\_addr\_1) : holds the register responsible for bits [15:8] of the memory address.

s8 - (mem\_addr\_2) : holds the register responsible for bits [23:16] of the memory address.

s9 - (mem\_addr\_read0) : holds the temporary data bits [7:0] of the memory address.

sA - (mem\_addr\_read1) : holds the temporary data bits [15:8] of the memory address.

sB - (mem\_addr\_read2) : holds the temporary data bits [23:16] of the memory address.

sC - (mem\_range\_selector) : variable that is set once the full memory has been reached (which starts displaying the entire memory locations now instead of comparing the mem\_addr\_read values to the current memory address.

## 7.1.7 Memory Map

read\_strobe[0x00] ;read in status of transmit engine

read\_strobe[0x01] ;read in received data from receive engine

write\_strobe[0x11] ;output Write Address Register 0

write\_strobe[0x12] ;Write Address Register 1

write\_strobe[0x13] ;Write Address Register 2

write\_strobe[0x14] ;Write Data Out Register 0

write\_strobe[0x15] ;Write Data Out Register 1

read\_strobe[0x16] ;Read Data In Register 0

read\_strobe[0x17] ;Read Data In Register 0

write\_strobe[0x18] ;Perform Memory Read

write\_strobe[0x19] ;Perform Memory Write

read\_strobe[0x1A] ;Read in Memory Interface Status

## 7.1.8 Memory Interface Block Verification

I verified that my I was my Memory Interface was corrct in two phases. First, I used the provided zip file that showed a model of the memory that we were using. I convinced myself that I was able to fully read and write from memory using the Micron Memory by simulating the provided testbench and making sure that I understood what was happening in the waveforms. After I verified this, I then made a top-level test bench where I made sure that everything was working correctly by using a simple test bench. In the Memory Interface test bench, I initialized my UART format to transfer at a baud rate of 460800 and have a format of 8O1. I then waited for the appropriate amount of time so that my test-bench would simulate sending my banner message and newline prompt. After that, I made sure that the receive engine correctly received the data of 0x5D. After I received the start bit from the receive data, I then waited for the bit time up to occur before I changed the Rx input value to the Receive Engine. This was so that I wasn't disturbing the Receive Engine while it was waiting for a bit time to begin collecting data. After a bit was shifted into the shift register, I then changed the Rx input in a way that would yield me receiving a byte of 0x5D. After all of the data bits were shifted into the shift register, I then loaded this data into a flop and sent the data to the PicoBlaze. As expected, the end result was that 0x5D was loaded into the flop and outputted to the PicoBlaze decoder (which selects what data is going to the In\_Port of the PicoBlaze). I also made sure that my Parity Error logic was correctly detecting a parity error by assigning the wrong parity to my byte of data. The 8O1 format should have an odd parity value of 0, but I gave the parity value a value of 1. As expected, The PARITY\_ERR status flag was set high and sent to the PicoBlaze decoder. I also made sure that all of my signals were changing correctly and that there were no surprises between the different states in my Receive Engine State Machine. After the character was successfully processed, I made sure that my state machine switched over to a Read operation and that the signals stayed consistent long enough for the Write operation to finish executing. After this, I repeated this process by sending in a value of 0xFF. After I successfully received this value, I then sent yet another value to the PicoBlaze, but this time it was an asterisk (which signals the PicoBlaze to read the data that has been saved to memory. This prompted my design to enter the Read state in my state machine. I made sure that all of my data signals going into my memory matched up to the expected values, and they did. I also made sure that the IOBUF was working as intended which it was. After observing that everything matched what I was expecting it to, I then concuded that my design was correct.

# 8. Chip Level Verification:

For the Chip Level Verification, I verified the chip via simulation by using a series of test benches to verify the correctness of my UART interface and Memory Interface Block. The discussion of what I did to verify my design can be found in sections 6.1.9 and 6.1.10.

# 9. Chip Level Test:

For the Chip Level test, I downloaded the project to a Nexys2 board and confirmed the correctness of my design. I did this by opening up a terminal window and then making sure that all of the UART communication data was similar. I then pushed reset on the Nexys2 board and this initialized the system. I then observed the banner being displayed on the terminal window and the command prompt being displayed as well. I then entered different characters on my keyboard and observed them being echoed onto the terminal (or performing the appropriate actions based on the chip requirements). After verifying the different character inputs and making sure that they accurately processed by the PicoBlaze, I then concluded that everything worked exactly as it was expected to.

# 10. Code:

-Starts on next page

Top Level:

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

//

// Author: Victor Espinoza

// Email: victor.alfonso94@gmail.com

// Project #: Project 5 - Memory Interface

// Course: CECS 460

//

// Create Date: 23:38:35 11/25/2015

//

// Module Name: proj5\_Memory\_Interface

// File Name: proj5\_Memory\_Interface.v

//

// Description: This top\_level module basically ties in all of the other

// modules that I made and connects them together. It takes the

// primary inputs of clk, rstb, bit8, parity\_en, odd\_n\_even,

// baud\_val[3:0], and Rx. This project has one output called tx.

// This tx output goes to P9, which is a port that connects to

// the RS-232 serial connector that connects to a UART terminal

// on a computer via a serial cable. The clk input comes from the

// clock on the Nexys 2 board, while the rstb input is a push

// button. The bit8, parity\_en, odd\_n\_even, and baud\_val[3:0]

// inputs are all switches on the Nexys 2 board. The rstb input

// is synchronized and distributed to all of the other modules in

// this project. This synchronized rstb value (rstbs) is also

// negated and then used as the reset input to the PicoBlaze

// processor. Inside of the PicoBlaze, I display my banner and

// my newline prompt and I then wait for a byte of data to be

// received by checking the RxRdy bit in the status register.

// Once the RxRdy bit is set, I then know that the Receive Engine

// has received a byte and is ready to receive another byte. I

// then load the received byte into a flop and send that data to

// a decoder (which uses read[0] to determine whether I am

// reading in the status of the UART engine or reading in the

// received data. I then output the received byte of data to the

// PicoBlaze. On the second clk cycle of the output instruction,

// I decode the Write\_Strobe value by using the Write\_Strobe and

// the Port\_Id port of the picoblaze. I then put these values

// into my write[255:0] register (because there are 2^8 registers

// that can be written to the PicoBlaze: 00 - FF). For my design,

// I output my values to the Port\_ID of 01, so I needed to pass

// my write[1] value into my transmit engine to let it know

// that it should load in the appropriate data bits (Out\_Port)

// into the shift register. I use the same logic flow for the

// Read\_Strobe (I have a read[255:0] register and I use read[0]

// and read[1] in my design. read[0] is used to read in the

// status flags to the PicoBlaze while read[1] is used to

// notify the Receive Engine that it is going to receive the

// data coming from the terminal window. The baud\_val[3:0] bits

// determine the baud rate at which the Program is going to be

// receiving and transmitting characters. The bit8, parity\_en and

// odd\_n\_even inputs determine the format of the data bits being

// received and transmitted (7N1, 7E1, 7O1, 8N1, 8O1, and 8E1).

// All of these inputs (minus the Rx input) go into my Transmit

// Engine where I update my shift register and baud

// counter accordingly. These inputs (including the Rx input)

// also go into my Receive Engine where I shift in the data one

// bit at a time. Once I establish the desired baud rate

// and data format, I then open a terminal window under the same

// baud rate and data format and then I am ready to start

// receiving/transmitting characters to the UART terminal. In

// the PicoBlaze I display my banner and then I transmit my

// prompt (\*>). I then wait to receive a character from the

// terminal, where I then process the data and either

// issue a newline command and a new prompt (carriage return

// or newline characters), display my hometown (asterisk

// character), delete the previous character (delete/

// backspace character), or echo the character. I also added my

// Seven-Segment display to this lab so that I can display

// my character counter value on the upper 2 Seven-Segment

// displays and the data being received by the Receive Engine

// in the lower 2 Seven-Segment displays. This helped me out

// tremendously in verifying that I was receiving the proper

// character data. Whenever a character is received from the

// terminal, I also save it to memory. To achieve this I

// need three registers to retrive the whole memory

// address (because the PicoBlaze only outputs 8-bits of

// data at a time and the memory address is 23 bits wide).

// Each register is updated with the out\_port value of the

// PicoBlaze only when its appropriate write\_strobe data is set

// high. These three registers are then concatenated and go into

// an OBUF, where they are outputted and mapped to the address

// pin locations for the Micron memory. I also need two additional

// 8-bit registers to hold in the input data that is going to be

// written into memory (the memory data is 16-bits wide which is

// why I need two 8-bit registers). Like the address registers,

// each write data out register is only updated when its

// appropriate write\_strobe number is set high. Finally, I have

// two additional 8-bit registers (read data in registers) that

// hold the data values that are outputted by the specific memory

// address. These two registers are only updated once a Read

// operation from memory has successfully been completed. Both of

// the write data out registers are concatenated and go into the

// input of an IOBUF while the a 16-bit wire called rdDataIn goes

// to the output of the IOBUF. The read data in registers are

// updated with the correct values located inside of the rdDataIn

// 16-bit wire once a Read operation has finished executing in

// the Memory.

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module proj5\_Memory\_Interface(clk, rstb, bit8, parity\_en, odd\_n\_even, baud\_val,

Rx, tx, a, b, c, d, e, f, g, a3, a2, a1, a0, LED, memWriteAddr, memoryData,

MT\_CLK, MT\_ADV, MT\_UB, MT\_LB, MT\_OE, MT\_WE, MT\_CE, MT\_CRE);

//Input and Output Declarations

input clk, rstb, bit8, parity\_en, odd\_n\_even, Rx;

input [3:0] baud\_val;

//memory address for micron memory

output MT\_CLK, MT\_ADV, MT\_UB, MT\_LB, MT\_OE;

output MT\_WE, MT\_CE, MT\_CRE;

wire MT\_CLK, MT\_ADV, MT\_UB, MT\_LB, MT\_OE;

wire MT\_WE, MT\_CE, MT\_CRE;

output [22:0] memWriteAddr;

wire [22:0] memWriteAddr;

//7-Segment Display info and tx output from transmit engine

output tx, a, b, c, d, e, f, g, a3, a2, a1, a0;

wire tx, a, b, c, d, e, f, g, a3, a2, a1, a0;

output [7:0] LED;

wire [7:0] LED;

//output data coming from micron memory

inout [15:0] memoryData;

wire [15:0] memoryData;

//Local Declarations

//wire rstsb, TxSet, TxRst, Done, sSet, sRst, ld, btu, shift;

wire rstsb, tx\_out, TxRdy, OE;

wire [7:0] in\_port, RxData;

wire [2:0] RxStatus;

wire interrupt, read\_strobe, write\_strobe, interrupt\_ack;

wire [7:0] out\_port;

wire [7:0] port\_id;

wire [15:0]rdDataIn;

wire memWrite, memRead;

wire [7:0] finalMemPicoData, memStatus;

reg [255:0] write, read;

//register variables

reg [7:0] charCounter, wrAddrReg0, wrAddrReg1, wrAddrReg2, memPicoData;

reg [7:0] wrDataOutReg0, wrDataOutReg1, rdDataInReg0, rdDataInReg1;

//state machine variables

reg RDY, ChipEnable, OutputEnable, WriteEnable, nOE, nReadLd, ReadLd;

reg nRDY, nChipEnable, nOutputEnable, nWriteEnable;

reg [1:0] present\_state, next\_state;

reg [2:0] sm\_clk\_counter;

wire sm\_clk\_pulse;

//symbolic state declaration

localparam [2:0]

idle = 2'b00,

performRead = 2'b01,

performWrite = 2'b10;

assign LED = {1'b0, bit8, parity\_en, odd\_n\_even, baud\_val[3:0]};

assign tx = tx\_out;

//synch\_reset module instantiation

//module synch\_reset(clk, rstb, rstsb);

synch\_reset Synchronizer\_Circuit(

.clk(clk),

.rstb(rstb),

.rstsb(rstsb)

);

//instantiate the RxStatusblaze

embedded\_kcpsm3 ekcp3(

.port\_id(port\_id),

.write\_strobe(write\_strobe),

.read\_strobe(read\_strobe),

.out\_port(out\_port),

.in\_port(in\_port),

.interrupt(interrupt),

.interrupt\_ack(interrupt\_ack),

.reset(!rstsb),

.clk(clk)

);

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//Chip Select for Transmit Engine, Receive Engine, and Memory Interface

//The write\_strobe and read\_strobe memory map is as follows:

//read\_strobe[0x00] ;read in status of transmit engine

//read\_strobe[0x01] ;read in received data from receive engine

//write\_strobe[0x11] ;output Write Address Register 0

//write\_strobe[0x12] ;Write Address Register 1

//write\_strobe[0x13] ;Write Address Register 2

//write\_strobe[0x14] ;Write Data Out Register 0

//write\_strobe[0x15] ;Write Data Out Register 1

//read\_strobe[0x16] ;Read Data In Register 0

//read\_strobe[0x17] ;Read Data In Register 0

//write\_strobe[0x18] ;Perform Memory Read

//write\_strobe[0x19] ;Perform Memory Write

//read\_strobe[0x1A] ;Read in Memory Interface Status

assign interrupt = 0;

//write strobe and read strobe decode

always@(\*)begin

write[255:0] = 256'b0;

write[port\_id] = write\_strobe;

read[255:0] = 256'b0;

read[port\_id] = read\_strobe;

end

assign memRead = write[24];

assign memWrite = write[25];

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//transmit\_engine module instantiation

//module transmit\_engine(clk, rstb, bit8, parity\_en, odd\_n\_even, baud\_val,

//txWrite, inData, tx, TxRdy);

transmit\_engine transmit(

.clk(clk),

.rstb(rstsb),

.bit8(bit8),

.parity\_en(parity\_en),

.odd\_n\_even(odd\_n\_even),

.baud\_val(baud\_val),

.txWrite(write[1]),

.inData(out\_port),

.tx(tx\_out),

.TxRdy(TxRdy)

);

//module receive\_engine(clk, rstb, bit8, parity\_en, odd\_n\_even, baud\_val, READ,

// Rx, status, data);

receive\_engine receive(

.clk(clk),

.rstb(rstsb),

.bit8(bit8),

.parity\_en(parity\_en),

.odd\_n\_even(odd\_n\_even),

.baud\_val(baud\_val),

.READ(read[1:0]),

.Rx(Rx),

.status(RxStatus),

.data(RxData)

);

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//Display Value Transmitted to Transmit Engine

always@(posedge clk, negedge rstsb)

if(!rstsb)

charCounter <= 8'b00;

else if (write[5])

charCounter <= out\_port;

else

charCounter <= charCounter;

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//Display Controller instantiation

//module display\_controller(clk, rstb, annode3, annode2, annode1, annode0,

// a3, a2, a1, a0, a, b, c, d, e, f, g);

display\_controller Display\_Controller(

.clk(clk),

.rstb(rstsb),

.annode3(charCounter[7:4]),

.annode2(charCounter[3:0]),

.annode1(RxData[7:4]),

.annode0(RxData[3:0]),

.a3(a3),

.a2(a2),

.a1(a1),

.a0(a0),

.a(a),

.b(b),

.c(c),

.d(d),

.e(e),

.f(f),

.g(g)

);

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//Write Address Registers

//Write Address Register 0

always@(posedge clk, negedge rstsb)

if(!rstsb)

wrAddrReg0 <= 8'b00;

else if (write[17])

wrAddrReg0 <= out\_port;

else

wrAddrReg0 <= wrAddrReg0;

//Write Address Register 1

always@(posedge clk, negedge rstsb)

if(!rstsb)

wrAddrReg1 <= 8'b00;

else if (write[18])

wrAddrReg1 <= out\_port;

else

wrAddrReg1 <= wrAddrReg1;

//Write Address Register 2

always@(posedge clk, negedge rstsb)

if(!rstsb)

wrAddrReg2 <= 8'b00;

else if (write[19])

wrAddrReg2 <= out\_port;

else

wrAddrReg2 <= wrAddrReg2;

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//Write Data Out Registers

//Write Data Out Register 0

always@(posedge clk, negedge rstsb)

if(!rstsb)

wrDataOutReg0 <= 8'b00;

else if (write[20])

wrDataOutReg0 <= out\_port;

else

wrDataOutReg0 <= wrDataOutReg0;

//Write Data Out Register 1

always@(posedge clk, negedge rstsb)

if(!rstsb)

wrDataOutReg1 <= 8'b00;

else if (write[21])

wrDataOutReg1 <= out\_port;

else

wrDataOutReg1 <= wrDataOutReg1;

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//Read Data In Registers

//Read Data In Register 0

always@(posedge clk, negedge rstsb)

if(!rstsb)

rdDataInReg0 <= 8'b00;

else if (ReadLd)

rdDataInReg0 <= rdDataIn[7:0];

else

rdDataInReg0 <= rdDataInReg0;

//Read Data In Register 1

always@(posedge clk, negedge rstsb)

if(!rstsb)

rdDataInReg1 <= 8'b00;

else if (ReadLd)

rdDataInReg1 <= rdDataIn[15:8];

else

rdDataInReg1 <= rdDataInReg1;

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//Assign the appropriate data going into the PicoBlaze Microcontroller

always @(\*)

case ({read[26], read[23], read[22]})

3'b001: memPicoData = rdDataInReg0; //Read Data In Register 0

3'b010: memPicoData = rdDataInReg1; //Read Data In Register 1

3'b100: memPicoData = memStatus; //Read Memory Status

default: memPicoData = 8'h00; //no bits

endcase

assign finalMemPicoData = memPicoData;

assign memStatus = {7'b0, RDY};

assign in\_port = (read[0]) ? {2'b0, RxStatus[2:1], 2'b0, TxRdy, RxStatus[0]} :

((read[1]) ? RxData : finalMemPicoData);

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//IOBUF and OBUF Instantiations

assign OE = nOE;

IOBUF iob[15:0](

.T(OE),

.I({wrDataOutReg1, wrDataOutReg0}),

.O(rdDataIn),

.IO(memoryData)

);

OBUF ob[22:0](

.I({wrAddrReg2[6:0], wrAddrReg1, wrAddrReg0}),

.O(memWriteAddr)

);

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//Finite State Machine for RX system

//The Memory Interface Block needs a Finite State Machine so that we can generate

//the appropriate signals to send to the CellRam module for a read and write

//operation to memory. The signals being generated are the chip enable,

//output enable, and the write enable. For a write operation, the chip enable will

//be set low and so will the write enable. Since the write enable has precedence

//over the output enable, I do not care what the output enable is so I set it high

//for the entirety of the write operation. For the read operation, I set the write

//enable high and set the chip enable and output enable variables low for the

//entirety of the read operation. Both the read and write operations take

//approximately 85ns to finish, so I hold the appropriate values stable for 5

//clock cycles (100ns) so that the data has enough time to finish. After those

//clock cycles are up, I then return the state machine to the idle state where

//it resets the signals to all be high and waits for the next operation to occur.

always@(posedge clk, negedge rstsb)begin

if(!rstsb)begin

present\_state <= idle;

//Reset outputs

{RDY, ChipEnable, OutputEnable, WriteEnable,ReadLd} <= 5'b11110;

end

else begin

present\_state <= next\_state; //update the present state

//update present outputs

{RDY, ChipEnable, OutputEnable, WriteEnable, ReadLd} <=

{nRDY, nChipEnable, nOutputEnable, nWriteEnable, nReadLd};

end

end

always@(\*)begin

next\_state = present\_state; //default state: the same

//wait for read or write

{nRDY, nChipEnable, nOutputEnable, nWriteEnable, nOE, nReadLd} = 6'b111110;

case(present\_state)

idle : begin

//update next states

{nRDY, nChipEnable, nOutputEnable, nWriteEnable, nOE, nReadLd}

= 6'b111110;

next\_state = (memRead) ? performRead : ((memWrite) ?

performWrite : idle);

end

performRead : begin

//update next states

{nRDY, nChipEnable, nOutputEnable, nWriteEnable, nOE} = 5'b00011;

next\_state = (sm\_clk\_pulse) ? idle : performRead;

nReadLd = (sm\_clk\_pulse) ? 1'b1 : 1'b0;

end

performWrite : begin

//update next states

{nRDY, nChipEnable, nOutputEnable, nWriteEnable, nReadLd} = 5'b00100;

next\_state = (sm\_clk\_pulse) ? idle : performWrite;

nOE = (WriteEnable);

end

default : begin

//update next states

{nRDY, nChipEnable, nOutputEnable, nWriteEnable, nOE, nReadLd}

= 6'b111100;

next\_state = idle;

end

endcase

end

//counter logic for counting for 5 clocks.

assign sm\_clk\_pulse = (sm\_clk\_counter == 4);

always@(posedge clk, negedge rstsb)

if(!rstsb)

sm\_clk\_counter <= 3'b0; //reset counter

else if (sm\_clk\_pulse)

sm\_clk\_counter <= 3'b0; //reset counter if pulse was achieved

else if (!ChipEnable)

sm\_clk\_counter <= sm\_clk\_counter + 1; //increment counter

else

sm\_clk\_counter <= 3'b0; //reset counter if in idle state

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//Assign outputs to micron memory

assign MT\_CLK = 1'b0; //always low according to project specs

assign MT\_ADV = 1'b0; //always low according to project specs

assign MT\_UB = 1'b0; //always low according to project specs

assign MT\_LB = 1'b0; //always low according to project specs

assign MT\_OE = OutputEnable;

assign MT\_WE = WriteEnable;

assign MT\_CE = ChipEnable;

assign MT\_CRE = 1'b0;

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

endmodule

Synchronizer Circuit:

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

//

// Author: Victor Espinoza

// Email: victor.alfonso94@gmail.com

// Project #: Project 3 - Transmit Engine plus PicoBlaze

// Course: CECS 460

// Create Date: 19:08:36 04/09/2015

//

// Module Name: synch\_reset

// File Name: synch\_reset.v

//

// Description: This is the Syncronization Circuit module that has an

// asynchronous input and a synchronous output. The purpose of this

// module is to take the asyncronous reset input and make it low-

// leveled active when pressed. This means that the reset value

// should be zero whenever the button is activated. When the reset

// button is pressed on the Nexys 2 board, its value comes into

// this module as the rstb input. However, in this module there are

// flip-flops that are designed with asynchronous (low active)

// resets. Also in this module, there is a synchronous reset that

// will neglect the asynchronous rstb input and force the 2

// flip-flops to zero at the posedge of the clock. This is how the

// rstb input turns from an input of 1 to an output of 0 and

// vice-versa. In other words, this is how the asynchronous rstb

// input turns into the synchronous rstsb output.

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module synch\_reset(clk, rstb, rstsb);

//Input and Output declarations

input clk, rstb;

output wire rstsb;

//local variables / flip-flop declarations

reg rst\_reg\_delay;

reg rst\_synch\_out;

assign rstsb = rst\_synch\_out;

always@(posedge clk, posedge rstb)begin

if(rstb)begin //force rstb to be low when activated instead of being high

rst\_reg\_delay <= 1'b0;

rst\_synch\_out <= 1'b0;

end

else begin //Synchronize the output

rst\_reg\_delay <= 1'b1;

rst\_synch\_out <= rst\_reg\_delay;

end

end

endmodule

PicoBlaze Processor:

////////////////////////////////////////////////////////////////////////////////

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////////////////////////////////////////////////////////////////////////////////

// \_\_\_\_ \_\_\_\_

// / /\/ /

// /\_\_\_/ \ / Vendor: Xilinx

// \ \ \/ Version: 1.01

// \ \ Filename: embedded\_kcpsm3.v

// / / Date Last Modified: 08/04/2004

// /\_\_\_/ /\ Date Created: 06/03/2003

// \ \ / \

// \\_\_\_\/\\_\_\_\

//

//Device: Xilinx

//Purpose:

// This file instantiates the KCPSM3 processor macro and connects the

// program ROM.

//Reference:

// None

//Revision History:

// Rev 1.00 - kc - Start of design entry in VHDL, 06/03/2003.

// Rev 1.01 - sus - Converted to verilog, 08/04/2004.

////////////////////////////////////////////////////////////////////////////////

// NOTE: The name of the program ROM will probably need to be changed to

// reflect the name of the program (PSM) file applied to the assembler.

////////////////////////////////////////////////////////////////////////////////

// Contact: e-mail picoblaze@xilinx.com

//////////////////////////////////////////////////////////////////////////////////

//

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// essential purpose of any limited remedies herein.

//////////////////////////////////////////////////////////////////////////////////

module embedded\_kcpsm3(

port\_id,

write\_strobe,

read\_strobe,

out\_port,

in\_port,

interrupt,

interrupt\_ack,

reset,

clk);

output[7:0] port\_id;

output write\_strobe;

output read\_strobe;

output[7:0] out\_port;

input[7:0] in\_port;

input interrupt;

output interrupt\_ack;

input reset;

input clk;

wire [7:0] port\_id;

wire write\_strobe;

wire read\_strobe;

wire [7:0] out\_port;

wire [7:0] in\_port;

wire interrupt;

wire interrupt\_ack;

wire reset;

wire clk;

wire [9:0] address;

wire [17:0] instruction;

//----------------------------------------------------------------------------------

//

// declaration of KCPSM3

//

//

// declaration of program ROM

//

//----------------------------------------------------------------------------------

//

// Start of test circuit description

//

kcpsm3 processor

( .address(address),

.instruction(instruction),

.port\_id(port\_id),

.write\_strobe(write\_strobe),

.out\_port(out\_port),

.read\_strobe(read\_strobe),

.in\_port(in\_port),

.interrupt(interrupt),

.interrupt\_ack(interrupt\_ack),

.reset(reset),

.clk(clk));

// uart\_rx program

// ( .address(address),

// .instruction(instruction),

// .clk(clk));

uart\_ful program

( .address(address),

.instruction(instruction),

.clk(clk));

endmodule

//----------------------------------------------------------------------------------

//

// END OF FILE EMBEDDED\_KCPSM3.V

//

//----------------------------------------------------------------------------------

Transmit Engine:

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

//

// Author: Victor Espinoza

// Email: victor.alfonso94@gmail.com

// Project #: Project 3 - Transmit Engine plus PicoBlaze

// Course: CECS 460

//

// Create Date: 11:37:29 10/15/2015

//

// Module Name: transmit\_engine

// File Name: transmit\_engine.v

//

// Description: My transmit engine module contains all of the logic needed to

// communicate with a computer via universal asynchronous

// receiver/transmitter (UART) communication. In order to create

// a stable UART connection, I needed to make sure that I could

// run my program at different baud rates and different data

// formats (7N1, 7O1, 7E1, 8N1, 8O1, 8E1). For this program, I

// am shifting out the data in 12-bit data packets. I use a

// shift register to determine what data gets shifted out. I am

// able to load in the data that is going to be shifted out

// by delaying the write[1] strobe from the PicoBlaze by 1 clock

// cycle (this is because the data on the out\_port of the

// PicoBlaze is not available until the next clock cycle). If

// my write1Delay variable is set high, I then load my shift

// register with the out\_port data of the PicoBlaze. I then

// update the remaining values in the shift register to make

// sure that I have accounted for the right parity, stop, and

// start bits. This is done using the bit8, parity\_en, and

// odd\_n\_even inputs. Once all of the data in the shift register

// is accurate, I then start shifting out the bits 1 bit at a

// time. I fill the most significant bit of my shift register

// with a 1 (which is equivalent to filling up the register

// with a bunch of stop bits). I keep track of when I am done

// shifting out all of the bits in my shift register by using

// a bit counter. In order to know when a bit is done being

// shifted out, I also needed to use a baud-rate counter.

// I first decoded the baud rate by reading in the data on my

// four baud\_rate switches. The next step was to determine what

// baud-rate I was running at based on those four switches. After

// determining the baud rate, I then needed to determine the

// amount of ticks I would need to achieve that specified baud-rate.

// I did this by using the formula baudCountNum = (1/baud rate) /

// (1/50MHz). This gave me the terminal count number that I needed

// to achieve the desired baud rate. I then assigned my baudCountNum

// variable to this terminal count. Once that value was reached, I

// then knew that I had finished transmitting one byte via UART

// communication. Now the next step was to increment my Bit Counter.

// I repeated this process until my Bit Counter reached 11, meaning

// that I had finished transmitting all 12 bits of data in the

// data packet. For this project, we are always going to end up

// transmitting 12 bits of data per data packet. That is why my

// bit time counter limit is always 11 (0 - (12-1)). Once all 12

// bits of data have been shifted out, I then set my Done variable

// to 1, which also sets my TxRdy variable to a 1. I then output

// this TxRdy variable, along with the other status variables

// to the PicoBlaze. These status variables are concatenated and

// represent the status register of the Transmit Engine. The

// TxRdy bit lets the PicoBlaze know that the Transmit Engine is

// ready to transmit another byte, at which point the PicoBlaze

// will output the next character being transmitted in the

// sequence to the Transmit Engine.

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module transmit\_engine(clk, rstb, bit8, parity\_en, odd\_n\_even, baud\_val, txWrite,

inData, tx, TxRdy);

//Input and Output Declarations

input clk, rstb, bit8, parity\_en, odd\_n\_even, txWrite;

input [3:0] baud\_val;

input [7:0] inData;

output tx;

output reg TxRdy;

//output transferLimit;

//Local Declarations

wire TxSet, TxRst, Done, sSet, sRst, ld, btu, shift;

reg [7:0] data;

//reg [6:0] transferLimitCounter;

reg [17:0] baudCountNum, baudCount, nBaudCount;

reg [3:0] bitCount, nBitCount;

reg start, write1Delay;

reg [11:0] sreg\_data;

reg b7, b8;

assign TxSet = Done;

assign TxRst = txWrite;

//R-S Flop that controlls the TxRdy input

//for the UART

always@(posedge clk, negedge rstb)

if(!rstb)

TxRdy <= 1'b1;

else if(TxSet)

TxRdy <= 1'b1;

else if(TxRst)

TxRdy <= 1'b0;

else

TxRdy <= TxRdy;

//assign pico\_data[7:0] = {6'b0, TxRdy, 1'b0};

assign sSet = txWrite;

assign sRst = Done;

//R-S Flop that controlls the start input

//for the UART

always@(posedge clk, negedge rstb)

if(!rstb)

start <= 1'b0;

else if(sSet)

start <= 1'b1;

else if(sRst)

start <= 1'b0;

else

start <= start;

assign ld = txWrite;

//register that holds the outport data

always@(posedge clk, negedge rstb)

if(!rstb)

data <= 8'b00;

else if (ld)

data <= inData;

else

data <= data;

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//Shift register logic

//register that delays the write strobe

//for one clock cycle

always@(posedge clk, negedge rstb)

if(!rstb)

write1Delay <= 1'b0;

else

write1Delay <= txWrite;

//logic used to determine b7 and b8 of the shift register (value changes

//depending on what bit8, parity\_en, and odd\_n\_even is).

always @(\*)

case ({bit8,parity\_en,odd\_n\_even})

3'b000: {b8,b7} = 2'b11; //7N1

3'b001: {b8,b7} = 2'b11; //7N1

3'b010: {b8,b7} = {1'b1, ^data[6:0]}; //7E1

3'b011: {b8,b7} = {1'b1, ~(^data[6:0])}; //7O1

3'b100: {b8,b7} = {1'b1, data[7]}; //8N1

3'b101: {b8,b7} = {1'b1, data[7]}; //8N1

3'b110: {b8,b7} = {(^data[7:0]), data[7]}; //8E1

3'b111: {b8,b7} = {~(^data[7:0]), data[7]}; //8O1

default: {b8,b7} = 2'b00; //no bits

endcase

//update shift register value uf write1Delay is set high

always @( posedge clk, negedge rstb)

if (!rstb)

sreg\_data <=12'hFFF; //load with all 1's

else if (write1Delay)

sreg\_data <= {1'b1,b8,b7,data[6:0], 1'b0, 1'b1};//load data into sreg

else if (shift)begin

sreg\_data <= sreg\_data >> 1; //shift data right by 1

sreg\_data [11] <= 1; //fill msb of shift register with a 1

end

assign tx = sreg\_data[0];

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//BAUD TIME COUNTER LOGIC:

//baud rate count decoder:

//values are derived using (1/baud rate) / (1/50MHz)

always@(\*)

case(baud\_val)

4'b0000: baudCountNum = 166667 -1; //300 BAUD Rate

4'b0001: baudCountNum = 41667 - 1; //1200 BAUD Rate

4'b0010: baudCountNum = 20833 - 1; //2400 BAUD Rate

4'b0011: baudCountNum = 10417 - 1; //4800 BAUD Rate

4'b0100: baudCountNum = 5208 - 1; //9600 BAUD Rate

4'b0101: baudCountNum = 2604 - 1; //19200 BAUD Rate

4'b0110: baudCountNum = 1302 - 1; //38400 BAUD Rate

4'b0111: baudCountNum = 868 - 1; //57600 BAUD Rate

4'b1000: baudCountNum = 434 - 1; //115200 BAUD Rate

4'b1001: baudCountNum = 217 - 1; //230400 BAUD Rate

4'b1010: baudCountNum = 109 - 1; //460800 BAUD Rate

4'b1011: baudCountNum = 54 - 1; //921600 BAUD Rate

default: baudCountNum = 166667 - 1; //300 BAUD Rate

endcase

//assign btu output tick and shift wire

assign btu = (baudCount == baudCountNum) ? 1'b1 : 1'b0;

assign shift = btu;

//Determine next state of baudCount

always@(\*)

case({btu, start})

2'b00 : nBaudCount = 18'b00;

2'b01 : nBaudCount = baudCount + 1;

2'b10 : nBaudCount = 18'b00;

2'b11 : nBaudCount = 18'b00;

default : nBaudCount = 18'b00;

endcase

//update baudCount accordingly

always @(posedge clk, negedge rstb)

if(!rstb) //check reset bit

baudCount <= 18'b0; //reset counter

else

baudCount <= nBaudCount; //update baudCount

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//BIT COUNTER LOGIC:

//For this lab we are always going to be transmitting 12 bits of data at a

//time. Once our counter has established that all 12 bits have been

//transmitted, we then set the Done variable high.

//assign Done output tick

assign Done = (bitCount == 11) ? 1'b1 : 1'b0;

//Determine next state of bitCount

always@(\*)

case({btu, start})

2'b00 : nBitCount = 4'b00;

2'b01 : nBitCount = (Done) ? 4'b00 : bitCount;

2'b10 : nBitCount = 4'b00;

2'b11 : nBitCount = bitCount + 1;

default : nBitCount = 4'b00;

endcase

//update bitCount accordingly

always @(posedge clk, negedge rstb)

if(!rstb) //check reset bit

bitCount <= 4'b0; //reset counter

else

bitCount <= nBitCount; //update bitCount

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

endmodule

Receive Engine:

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

//

// Author: Victor Espinoza

// Email: victor.alfonso94@gmail.com

// Project #: Project 4 - Full UART Engine

// Course: CECS 460

//

// Create Date: 11:37:29 10/15/2015

//

// Module Name: receive\_engine

// File Name: receive\_engine.v

//

// Description: My receive engine module contains all of the logic needed to

// receive information from a computer via universal asynchronous

// receiver/transmitter (UART) communication. In order to create

// a stable UART connection, I needed to make sure that I could

// run my program at different baud rates and different data

// formats (7N1, 7O1, 7E1, 8N1, 8O1, 8E1). For this program, I

// am shifting in the data from the receive engine 1-bit at a time.

// I use a shift register to store the receive engine data bits.

// Each data bit gets shifted in one bit at a time. For the receive

// engine we have a state diagram that consists of four different

// states: IDLE, S1, S2, and S3. The state machine starts off in

// the IDLE state at reset. In this state, it waits for a start bit

// (which is agreed to be a zero). We then move to the S1 state,

// where the state machine waits for half a bit-time. If the Rx

// input changes to a 1 during this half bit-time interval, I then

// move back to the IDLE state where we reset the bit-time interval

// and wait to receive a start bit value (0). If the Rx input

// stays the same (0) for the entirety of the half-bit time, this

// means that we actually received a start bit and I then move on to

// the next state, S2. I now know that we need to start collecting

// the data bits, so in S2, I wait wait for an entire bit time.

// After the bit time is achieved, I am know in the middle of the

// first data bit. I then move on to state S3, where I shift the

// data bit value into my shift register. I then check to see if

// all of the data bits have been shifted in to my shift register

// by checking the status of my bcu variable. This variable is set

// high for one clock cycle whenever all of the data bits have

// been received. If the bcu variable is set high, then I go back

// to the idle state where I wait until another bit is received.

// If the variable is not set high, then I go back to S2 and wait

// for another bit time so that I can shift in the next bit into

// the receive engine. Once all of the data bits have been

// shifted into the receive engine, I then send these data bits

// to the PicoBlaze so that it can process the received character

// and determine what to do with that data.

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module receive\_engine(clk, rstb, bit8, parity\_en, odd\_n\_even, baud\_val, READ,

Rx, status, data);

//Input and Output Declarations

input clk, rstb, bit8, parity\_en, odd\_n\_even, Rx;

input [1:0] READ;

input [3:0] baud\_val;

output [7:0] data;

output [2:0] status;

reg [7:0] data;

wire [2:0] status;

//Local Declarations

//symbolic state declaration

localparam [2:0]

idle = 2'b00,

state\_1 = 2'b01,

state\_2 = 2'b10,

state\_3 = 2'b11;

wire RxSet, RxRst, sSet, sRst, SEVEN, btu, bcu, done;//shift;

wire parSet, parRst;

reg START, DOIT, LOAD, nSTART, nDOIT, nLOAD;

wire [17:0] finalBaudCountNum;

reg [17:0] baudCountNum, baudCount, nBaudCount;

reg [3:0] bitCount, nBitCount;

reg [1:0] present\_state, next\_state;

reg RxRdy, OVERFLOW, doneDelay;

reg [8:0] sreg\_data;

wire b7, receivedParity, computedParity, generatedParity;

wire combinedParities, parityResult;

reg PARITY\_ERR;

assign RxSet = doneDelay & !RxRdy;

assign RxRst = READ[1];

//R-S Flop that controlls the RxRdy input

//for the UART

always@(posedge clk, negedge rstb)

if(!rstb)

RxRdy <= 1'b1;

else if(RxSet)

RxRdy <= 1'b1;

else if(RxRst)

RxRdy <= 1'b0;

else

RxRdy <= RxRdy;

assign sSet = LOAD & RxRdy;

assign sRst = READ[0];

//R-S Flop that controlls the overflow output

//for the UART

always@(posedge clk, negedge rstb)

if(!rstb)

OVERFLOW <= 1'b0;

else if(sSet)

OVERFLOW <= 1'b1;

else if(sRst)

OVERFLOW <= 1'b0;

else

OVERFLOW <= OVERFLOW;

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//Finite State Machine for RX system

//For the receive engine we have a state diagram that consists of four different

//states: IDLE, S1, S2, and S3. The state machine starts off in

//the IDLE state at reset. In this state, it waits for a start bit

//(which is agreed to be a zero). We then move to the S1 state,

//where the state machine waits for half a bit-time. If the Rx

//input changes to a 1 during this half bit-time interval, I then

//move back to the IDLE state where we reset the bit-time interval

//and wait to receive a start bit value (0). If the Rx input

//stays the same (0) for the entirety of the half-bit time, this

//means that we actually received a start bit and I then move on to

//the next state, S2. I now know that we need to start collecting

//the data bits, so in S2, I wait wait for an entire bit time.

//After the bit time is achieved, I am know in the middle of the

//first data bit. I then move on to state S3, where I shift the

//data bit value into my shift register. I then check to see if

//all of the data bits have been shifted in to my shift register

//by checking the status of my bcu variable. This variable is set

//high for one clock cycle whenever all of the data bits have

//been received. If the bcu variable is set high, then I go back

//to the idle state where I wait until another bit is received.

//If the variable is not set high, then I go back to S2 and wait

//for another bit time so that I can shift in the next bit into

//the receive engine. Once all of the data bits have been

//shifted into the receive engine, I then send these data bits

//to the PicoBlaze so that it can process the received character

//and determine what to do with that data.

always@(posedge clk, negedge rstb)begin

if(!rstb)begin

present\_state <= idle;

{START, DOIT, LOAD} <= 3'b000; //Reset outputs

end

else begin

present\_state <= next\_state; //update the present state

{START, DOIT, LOAD} <= {nSTART, nDOIT, nLOAD}; //update present outputs

end

end

always@(\*)begin

next\_state = present\_state; //default state: the same

{nSTART, nDOIT, nLOAD} = 3'b000; //wait for start bit

case(present\_state)

idle : begin

{nSTART, nDOIT, nLOAD} = 3'b000; //wait for start bit

next\_state = (Rx) ? idle : state\_1;

end

state\_1 : begin

{nSTART, nDOIT, nLOAD} = 3'b110; //wait for half bit-time

next\_state = (Rx) ? idle : ((btu) ? state\_2 : state\_1 );

end

state\_2 : begin

{nSTART, nDOIT, nLOAD} = 3'b010; //wait for full bit-time

next\_state = (btu) ? state\_3 : state\_2;

end

state\_3 : begin

{nSTART, nDOIT, nLOAD} = 3'b011; //load bit into shift register

next\_state = (bcu) ? idle : state\_2;

end

default : begin

{nSTART, nDOIT, nLOAD} = 3'b000; //wait for start bit

next\_state = idle;

end

endcase

end

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//update shift register value until it contains all of the receive data

always @(posedge clk, negedge rstb)

if (!rstb)

sreg\_data <=9'hFFF; //load with all 1's

else if (!START & !DOIT & !LOAD)

sreg\_data <=9'hFFF; //load with all 1's

else if (LOAD & !START)begin

sreg\_data <= sreg\_data >> 1; //shift data right by 1

sreg\_data [8] <= Rx; //fill msb of shift register with Rx input

end

assign SEVEN = !bit8;

//generate the parity error result

assign b7 = (SEVEN) ? 1'b0 : sreg\_data[7];

assign receivedParity = (SEVEN) ? sreg\_data[7] : sreg\_data[8];

assign computedParity = ^{b7,sreg\_data[6:0]};

assign generatedParity = (odd\_n\_even) ? ~computedParity : computedParity;

assign combinedParities = ^{receivedParity, generatedParity};

assign parityResult = doneDelay & parity\_en & combinedParities;

assign parSet = parityResult;

assign parRst = READ[0];

//R-S Flop that controlls the Parity Error output for the UART

always@(posedge clk, negedge rstb)

if(!rstb)

PARITY\_ERR <= 1'b0;

else if(parSet)

PARITY\_ERR <= 1'b1;

else if(parRst)

PARITY\_ERR <= 1'b0;

else

PARITY\_ERR <= PARITY\_ERR;

//data to picoblaze

always @(posedge clk, negedge rstb)

if(!rstb)

data <= 8'b0;

else if (doneDelay)

data <= {b7, sreg\_data[6:0]};

//status to picoblaze

assign status = {OVERFLOW, PARITY\_ERR, RxRdy};

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//BAUD TIME COUNTER LOGIC:

//baud rate count decoder:

//values are derived using (1/baud rate) / (1/50MHz)

always@(\*)

case(baud\_val)

4'b0000: baudCountNum = 166667 -1; //300 BAUD Rate

4'b0001: baudCountNum = 41667 - 1; //1200 BAUD Rate

4'b0010: baudCountNum = 20833 - 1; //2400 BAUD Rate

4'b0011: baudCountNum = 10417 - 1; //4800 BAUD Rate

4'b0100: baudCountNum = 5208 - 1; //9600 BAUD Rate

4'b0101: baudCountNum = 2604 - 1; //19200 BAUD Rate

4'b0110: baudCountNum = 1302 - 1; //38400 BAUD Rate

4'b0111: baudCountNum = 868 - 1; //57600 BAUD Rate

4'b1000: baudCountNum = 434 - 1; //115200 BAUD Rate

4'b1001: baudCountNum = 217 - 1; //230400 BAUD Rate

4'b1010: baudCountNum = 109 - 1; //460800 BAUD Rate

4'b1011: baudCountNum = 54 - 1; //921600 BAUD Rate

default: baudCountNum = 166667 - 1; //300 BAUD Rate

endcase

//The START signal determines whether I am counting for a full bit time

//or half of a bit time. When START is high, I assign the count value to

//half of the original value (by shifting it to the right once). This

//means that I am looking for the start bit of the received data (0)

//and as a result I am only waiting for half of a bit-time. When START

//is low, I assign te count value to the original value (meaning that I

//am waiting for a full bit-time).

assign finalBaudCountNum = (START) ? (baudCountNum >> 1) : baudCountNum;

//assign btu output tick and shift wire

assign btu = (baudCount == finalBaudCountNum) ? 1'b1 : 1'b0;

//assign shift = btu;

//Determine next state of baudCount

always@(\*)

case({btu, DOIT})

2'b00 : nBaudCount = 18'b00;

2'b01 : nBaudCount = baudCount + 1;

2'b10 : nBaudCount = 18'b00;

2'b11 : nBaudCount = 18'b00;

default : nBaudCount = 18'b00;

endcase

//update baudCount accordingly

always @(posedge clk, negedge rstb)

if(!rstb) //check reset bit

baudCount <= 18'b0; //reset counter

else

baudCount <= nBaudCount; //update baudCount

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//BIT COUNTER LOGIC:

//For this lab we are always going to be transmitting 12 bits of data at a

//time. Once our counter has established that all 12 bits have been

//transmitted, we then set the Done variable high.

//assign Done output tick

assign bcu = (bitCount == 11) ? 1'b1 : 1'b0;

assign done = bcu;

//Determine next state of bitCount

always@(\*)

case({btu, DOIT})

2'b00 : nBitCount = 4'b00;

2'b01 : nBitCount = (done) ? 4'b00 : bitCount;

2'b10 : nBitCount = 4'b00;

2'b11 : nBitCount = bitCount + 1;

default : nBitCount = 4'b00;

endcase

//update bitCount accordingly

always @(posedge clk, negedge rstb)

if(!rstb) //check reset bit

bitCount <= 4'b0; //reset counter

else

bitCount <= nBitCount; //update bitCount

//done delay (allows time to load the bit into the shift register)

always@(posedge clk, negedge rstb)

if(!rstb) //check reset bit

doneDelay <= 1'b0;

else

doneDelay <= done;

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

endmodule

Display Controller

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

//

// Author: Victor Espinoza

// Email: victor.alfonso94@gmail.com

// Project #: Project 2 - PicoBlaze Integration with Interrupts

// Course: CECS 460

// Create Date: 13:19:08 04/18/2015

//

// Module Name: top\_level

// File Name: top\_level.v

//

// Description: This Display Controller module controls the 7-Segment display

// and everything that it needs in order to correctly display

// the appropriate values. This module was created in Professor

// Allison's CECS 301 class. Each section of this module is

// described within the module itself using comments.

//

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module display\_controller(clk, rstb, annode3, annode2, annode1, annode0,

a3, a2, a1, a0, a, b, c, d, e, f, g);

//Input and Output Declarations

input clk, rstb;

input [3:0] annode3, annode2, annode1, annode0;

//annode and cathode variables for the 7-Segment Display

output reg a, b, c, d, e, f, g;

output wire a3, a2, a1, a0;

//Local Variables

reg [3:0] ad\_out;

wire [1:0] seg\_sel;

reg clk\_250;

//counter variable

reg [15:0] count = 0;

//initialize LED clock:

//Divide 50MHz on-board clock to 250Hz. This is done so that

//it appears to the human observer that all four anode signals

//are on even when in reality they are not. This is done by

//driving the cathode patterns at least once every 16ms,

//which comes out to 4ms per annode/cathode pattern.

always @(posedge clk, negedge rstb)

//if rstb then rstb count and clock

if(!rstb) begin

count <= 0;

clk\_250 <= 0;

end

else begin

//increment count

count <= (count + 1);

//set output clock to opposite if count is greater than or equal to 25000

if(count >= 25000) begin

count <= 0;

clk\_250 <= ~clk\_250;

end

end

//initialize LED controller module:

//module led\_controller(clk, rstb, a3, a2, a1, a0, seg\_sel);

led\_controller LED\_contr(

.clk(clk\_250),

.rstb(rstb),

.a3(a3),

.a2(a2),

.a1(a1),

.a0(a0),

.seg\_sel(seg\_sel)

);

//initialize address mux:

//This multiplexer is used to select what data input is to

//be assigned to the ad\_out output and driven to the seven segment

//display. The value of the ad\_out is chosen based on the seg\_sel

//input that was generated by our led\_controller module.

always @(seg\_sel, annode3, annode2, annode1, annode0)

case (seg\_sel)

2'b00 : ad\_out = annode0; //annode 0

2'b01 : ad\_out = annode1; //annode 1

2'b10 : ad\_out = annode2; //annode 2

2'b11 : ad\_out = annode3; //annode 3

default: ad\_out = 4'bx; //default output

endcase

//initialize hex to seven segment display

//This hex\_to\_7segment module basicaly takes in a four bit input

//and depending on what that input is, it then transfers that

//information by turning on the appropriate segments (a-g) on the

//seven segment display in order to represent that four bit input.

//This was achieved by using case statements for all of the

//appropriate 4-bit input options and assigning the according

//values for a-g for that 4-bit input. Depending on the 4-bit

//value, the appropriate segments are turned on in order to

//display that value.

always@(ad\_out)

case (ad\_out)

4'b0000: {a, b, c, d, e, f, g} = 7'b0000001; //Display 0

4'b0001: {a, b, c, d, e, f, g} = 7'b1001111; //Display 1

4'b0010: {a, b, c, d, e, f, g} = 7'b0010010; //Display 2

4'b0011: {a, b, c, d, e, f, g} = 7'b0000110; //Display 3

4'b0100: {a, b, c, d, e, f, g} = 7'b1001100; //Display 4

4'b0101: {a, b, c, d, e, f, g} = 7'b0100100; //Display 5

4'b0110: {a, b, c, d, e, f, g} = 7'b0100000; //Display 6

4'b0111: {a, b, c, d, e, f, g} = 7'b0001111; //Display 7

4'b1000: {a, b, c, d, e, f, g} = 7'b0000000; //Display 8

4'b1001: {a, b, c, d, e, f, g} = 7'b0001100; //Display 9

4'b1010: {a, b, c, d, e, f, g} = 7'b0001000; //Display A

4'b1011: {a, b, c, d, e, f, g} = 7'b1100000; //Display B

4'b1100: {a, b, c, d, e, f, g} = 7'b0110001; //Display C

4'b1101: {a, b, c, d, e, f, g} = 7'b1000010; //Display D

4'b1110: {a, b, c, d, e, f, g} = 7'b0110000; //Display E

4'b1111: {a, b, c, d, e, f, g} = 7'b0111000; //Display F

default: {a, b, c, d, e, f, g} = 7'b1111111; //Display Nothing

endcase

endmodule

LED Controller:

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

//

// Author: Victor Espinoza

// Email: victor.alfonso94@gmail.com

// Project #: Project 2 - PicoBlaze Integration with Interrupts

// Course: CECS 460

// Create Date: 20:10:05 10/12/2013

//

// Module Name: led\_controller

// File Name: led\_controller.v

//

// Description: This is an LED controller based on Professor Allison's CECS

// 301 class. The purpose of this module is to choose which

// anodes on the 7-segment displays are asserted and when they

// should be asserted. This is determined according to the LED

// clock within the Display Controller module.

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module led\_controller(clk, rstb, a3, a2, a1, a0, seg\_sel);

//Input and Output Declarations

input clk, rstb;

output reg a3, a2, a1, a0;

output reg [1:0] seg\_sel;

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// state register and next\_state variables

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

reg [1:0] present\_state;

reg [1:0] next\_state;

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Next State Combinational Logic

//(next state values can change anytime but will only be "clocked" below)

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

always @(present\_state)

case (present\_state)

//next state combinations for present states

2'b00 : next\_state = 2'b01;

2'b01 : next\_state = 2'b10;

2'b10 : next\_state = 2'b11;

2'b11 : next\_state = 2'b00;

//next state combinations for all other present states

default: next\_state = 2'b00;

endcase

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// State Register Logic (Sequential Logic)

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

always @(posedge clk, negedge rstb)

if (!rstb)

//Got a rstb, so set state register to all 0's

present\_state <= 2'b00;

else

//Got a posedge, so update state register with next state

present\_state <= next\_state;

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Output Combinational Logic and Segment Select Logic

//(output values can change only when a present state changes)

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

always @(present\_state)

case (present\_state)

//output combinations for present states

2'b00 : {seg\_sel, a3, a2, a1, a0} = 6'b00\_1110; //a[0] seg\_sel asserted

2'b01 : {seg\_sel, a3, a2, a1, a0} = 6'b01\_1101; //a[1] seg\_sel asserted

2'b10 : {seg\_sel, a3, a2, a1, a0} = 6'b10\_1011; //a[2] seg\_sel asserted

2'b11 : {seg\_sel, a3, a2, a1, a0} = 6'b11\_0111; //a[3] asserted

//output combinations for all other present states

default : {seg\_sel, a3, a2, a1, a0} = 6'b00\_1110;

endcase

endmodule

UCF File:

//Set the appropriate step and rstb

//clk input

NET "clk" LOC="B8";

//button inputs

NET "rstb" LOC="B18";

NET "tx" LOC="P9";

NET "Rx" LOC="U6";

//NET "rx" LOC="V6";

#NET "parity\_en" LOC="N17";

#NET "odd\_n\_even" LOC="L13";

#NET "bit8" LOC="L14";

NET "bit8" LOC="N17";

NET "parity\_en" LOC="L13";

NET "odd\_n\_even" LOC="L14";

NET "baud\_val[3]" LOC="K17";

NET "baud\_val[2]" LOC="K18";

NET "baud\_val[1]" LOC="H18";

NET "baud\_val[0]" LOC="G18";

//annode and cathode info for the 7

//segment display

NET "a3" LOC="F15"| IOSTANDARD = LVCMOS33;

NET "a2" LOC="C18"| IOSTANDARD = LVCMOS33;

NET "a1" LOC="H17"| IOSTANDARD = LVCMOS33;

NET "a0" LOC="F17"| IOSTANDARD = LVCMOS33;

NET "a" LOC= "L18"| IOSTANDARD = LVCMOS33;

NET "b" LOC= "F18"| IOSTANDARD = LVCMOS33;

NET "c" LOC= "D17"| IOSTANDARD = LVCMOS33;

NET "d" LOC= "D16"| IOSTANDARD = LVCMOS33;

NET "e" LOC= "G14"| IOSTANDARD = LVCMOS33;

NET "f" LOC= "J17"| IOSTANDARD = LVCMOS33;

NET "g" LOC= "H14"| IOSTANDARD = LVCMOS33;

NET "LED[7]" LOC= "R4"| IOSTANDARD = LVCMOS33;

NET "LED[6]" LOC= "F4"| IOSTANDARD = LVCMOS33;

NET "LED[5]" LOC= "P15"| IOSTANDARD = LVCMOS33;

NET "LED[4]" LOC= "E17"| IOSTANDARD = LVCMOS33;

NET "LED[3]" LOC= "K14"| IOSTANDARD = LVCMOS33;

NET "LED[2]" LOC= "K15"| IOSTANDARD = LVCMOS33;

NET "LED[1]" LOC= "J15"| IOSTANDARD = LVCMOS33;

NET "LED[0]" LOC= "J14"| IOSTANDARD = LVCMOS33;

Top Level Test Bench:

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

//

// Author: Victor Espinoza

// Email: victor.alfonso94@gmail.com

// Project #: Project 5 - Memory Interface

// Course: CECS 460

//

// Create Date: 23:38:35 11/25/2015

//

// Module Name: proj\_5\_Memory\_Interface\_tb

// File Name: proj\_5\_Memory\_Interface\_tb.v

//

// Description: I verified that my I was my Memory Interface was corrct in two

// phases. First, I used the provided zip file that showed a model

// of the memory that we were using. I convinced myself that I was

// able to fully read and write from memory using the Micron Memory

// by simulating the provided testbench and making sure that I

// understood what was happening in the waveforms. After I verified

// this, I then made a top-level test bench where I made sure that

// everything was working correctly by using a simple test bench.

// In the Memory Interface test bench, I initialized my UART format

// to transfer at a baud rate of 460800 and have a format of 8O1.

// I then waited for the appropriate amount of time so that my

// test-bench would simulate sending my banner message and newline

// prompt. After that, I made sure that the receive engine correctly

// received the data of 0x5D. After I received the start bit from

// the receive data, I then waited for the bit time up to occur

// before I changed the Rx input value to the Receive Engine. This

// was so that I wasn't disturbing the Receive Engine while it was

// waiting for a bit time to begin collecting data. After a bit was

// shifted into the shift register, I then changed the Rx input in

// a way that would yield me receiving a byte of 0x5D. After all of

// the data bits were shifted into the shift register, I then loaded

// this data into a flop and sent the data to the PicoBlaze. As

// expected, the end result was that 0x5D was loaded into the flop

// and outputted to the PicoBlaze decoder (which selects what data is

// going to the In\_Port of the PicoBlaze). I also made sure that my

// Parity Error logic was correctly detecting a parity error by

// assigning the wrong parity to my byte of data. The 8O1 format

// should have an odd parity value of 0, but I gave the parity value

// a value of 1. As expected, The PARITY\_ERR status flag was set high

// and sent to the PicoBlaze decoder. I also made sure that all of my

// signals were changing correctly and that there were no surprises

// between the different states in my Receive Engine State Machine.

// After the character was successfully processed, I made sure that

// my state machine switched over to a Read operation and that the

// signals stayed consistent long enough for the Write operation to

// finish executing. After this, I repeated this process by sending

// in a value of 0xFF. After I successfully received this value, I

// then sent yet another value to the PicoBlaze, but this time it

// was an asterisk (which signals the PicoBlaze to read the data that

// has been saved to memory. This prompted my design to enter the

// Read state in my state machine. I made sure that all of my data

// signals going into my memory matched up to the expected values, and

// they did. I also made sure that the IOBUF was working as intended

// which it was. After observing that everything matched what I was

// expecting it to, I then concuded that my design was correct.

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module proj\_5\_Memory\_Interface\_tb;

//Inputs

reg clk;

reg rstb;

reg bit8;

reg parity\_en;

reg odd\_n\_even;

reg [3:0] baud\_val;

reg Rx;

wire Tx;

wire [22:0] memWriteAddr;

wire [15:0] memoryData;

wire MT\_CLK, MT\_ADV, MT\_UB, MT\_LB, MT\_OE, MT\_WE, MT\_CE, MT\_CRE;

//Instantiate the Unit Under Test (UUT)

//module proj5\_Memory\_Interface(clk, rstb, bit8, parity\_en, odd\_n\_even, baud\_val,

//Rx, tx, a, b, c, d, e, f, g, a3, a2, a1, a0, LED, memWriteAddr, memoryData,

//MT\_CLK, MT\_ADV, MT\_UB, MT\_LB, MT\_OE, MT\_WE, MT\_CE, MT\_CRE);

proj5\_Memory\_Interface uut(

.clk(clk),

.rstb(rstb),

.bit8(bit8),

.parity\_en(parity\_en),

.odd\_n\_even(odd\_n\_even),

.baud\_val(baud\_val),

.Rx(Rx),

.tx(Tx),

.memWriteAddr(memWriteAddr),

.memoryData(memoryData),

.MT\_CLK(MT\_CLK),

.MT\_ADV(MT\_ADV),

.MT\_UB(MT\_UB),

.MT\_LB(MT\_LB),

.MT\_OE(MT\_OE),

.MT\_WE(MT\_WE),

.MT\_CE(MT\_CE),

.MT\_CRE(MT\_CRE)

);

//vary the clk signal every 10ns to mimick a

//period of 20ns (which is the period of our boards)

always #10 clk = ~clk;

//always #20 tx\_Write = ~tx\_Write;

initial begin

//Initialize Inputs

clk = 0;

rstb = 1; //low active reset

//8O1 (300 Baud) Transmitting 0x65 = 110\_0101

bit8 = 1; //8 bits of data

parity\_en = 1; //parity enabled

odd\_n\_even = 1; //odd parity

baud\_val = 4'hA; //baud = 460800 BAUD Rate

Rx = 1'b1; //data to be transmitted

//Wait 100 ns for global reset to finish

#100 @(posedge clk) rstb = 0; // have reset become unactive.

#3500000 @(posedge clk)

Rx = 1'b0; //data to be transmitted

//Receive 0x5D

//d0

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b1;

//d1

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b0;

//d2

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b1;

//d3

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b1;

//d4

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b1;

//d5

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b0;

//d6

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b1;

//d7

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b0;

//parity/stop

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b1;

wait (uut.receive.done == 1); //wait until byte is done being received.

wait (uut.receive.done == 0);

#500000 @(posedge clk)

Rx = 1'b0; //data to be transmitted

//Receive 0xFF

//d0

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b1;

wait (uut.receive.done == 1); //wait until byte is done being received.

wait (uut.receive.done == 0);

#500000 @(posedge clk)

Rx = 1'b0; //data to be transmitted

//Receive 0x2A = 0010 1010

//d0

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b0;

//d0

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b0;

//d1

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b1;

//d2

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b0;

//d3

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b1;

//d4

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b0;

//d5

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b1;

//d6

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b0;

//d7

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b0;

//parity/stop

wait (uut.receive.btu == 1);

wait (uut.receive.btu == 0);

Rx = 1'b1;

wait (uut.receive.done == 1); //wait until byte is done being received.

wait (uut.receive.done == 0);

#1000000

$stop;

end

endmodule

Cell Ram Testbench

// Testbench for CellularRAM

// DO NOT CHANGE THE TIMESCALE

// MAKE SURE YOUR SIMULATOR USE "PS" RESOLUTION

`timescale 1ns / 1ps

module tb;

`include "cellram\_parameters.vh"

parameter tDS = tDW;

parameter WAIT\_LIMIT = 1000;

// ports

reg clk;

reg adv\_n;

reg cre;

reg ce\_n;

reg oe\_n;

reg we\_n;

reg [BY\_BITS-1:0] by\_n;

reg [31:0] addr;

wire [31:0] dq;

wire [DQ\_BITS-1:0] dq\_in = dq;

// configuration registers

reg [DQ\_BITS-1:0] bus\_configuration\_reg;

reg [DQ\_BITS-1:0] refr\_configuration\_reg;

wire waitp = bus\_configuration\_reg[10];

wire [3:0] latency\_counter = (bus\_configuration\_reg[13:11] == 3'b000) ? 4'd8 : bus\_configuration\_reg[13:11];

// dq transmit

reg [DQ\_BITS-1:0] dq\_out;

assign dq = {{32-DQ\_BITS{1'bz}}, dq\_out};

// dq receive

reg [BY\_BITS-1:0] rd\_dm;

reg [DQ\_BITS-1:0] rd\_dq;

reg rd\_comp;

realtime tm\_rd\_comp;

wire o\_wait;

wire i\_wait = waitp ? o\_wait : ~o\_wait;

// timing definition

realtime tclk;

realtime tclk\_min;

initial begin

$timeformat (-9, 1, " ns", 1);

`ifdef period

tclk = `period ;

`else

tclk = tCLK;

`endif

end

// component instantiation

cellram uut (

.clk (clk),

.adv\_n (adv\_n),

.cre (cre),

.o\_wait (o\_wait),

.ce\_n (ce\_n),

.oe\_n (oe\_n),

.we\_n (we\_n),

.ub\_n (by\_n[1]),

.lb\_n (by\_n[0]),

.addr (addr[ADDR\_BITS-1:0]),

.dq (dq[DQ\_BITS-1:0])

);

function integer ceil;

input number;

real number;

if (number > $rtoi(number))

ceil = $rtoi(number) + 1;

else

ceil = number;

endfunction

function integer max;

input arg1;

input arg2;

integer arg1;

integer arg2;

if (arg1 > arg2)

max = arg1;

else

max = arg2;

endfunction

task clk\_pulse;

input [31:0] count;

integer i;

begin

for (i=0; i<count; i=i+1) begin

clk <= #(i\*tclk) 1'b0;

clk <= #((i + 0.5)\*tclk) 1'b1;

end

end

endtask

task set\_config\_reg\_copy;

input [1:0] regnum;

input [DQ\_BITS-1:0] regval;

begin

case (regnum)

BCR : bus\_configuration\_reg = regval;

RCR : refr\_configuration\_reg = regval;

endcase

tclk\_min = min\_clk\_period(bus\_configuration\_reg[14], bus\_configuration\_reg[13:11]);

end

endtask

task power\_up;

begin

clk = 1'b0;

adv\_n = 1'b1;

cre = 1'b0;

ce\_n = 1'b1;

oe\_n = 1'b1;

we\_n = 1'b1;

by\_n = {BY\_BITS{1'b1}};

dq\_out= {DQ\_BITS{1'bz}};

addr= {32{1'bz}};

#(tPU);

end

endtask

task async\_write;

input wr\_cre;

input [ADDR\_BITS-1:0] wr\_addr;

input [DQ\_BITS-1:0] wr\_data;

input [BY\_BITS-1:0] wr\_byte;

input wr\_adv;

begin

clk <= 1'b0;

adv\_n <= 1'b0;

cre <= wr\_cre;

ce\_n <= 1'b0;

oe\_n <= 1'b1;

we\_n <= 1'b1;

if (GENERATION == CR20) begin

we\_n <= #(tVP - tAVS + tAS) 1'b0;

end else begin

we\_n <= #(tWC - tWP) 1'b0;

end

by\_n <= wr\_byte;

addr <= wr\_addr;

dq\_out <= #(tCW - tDS) wr\_data;

dq\_out <= #(tCW + tDH) {DQ\_BITS{1'bz}};

if (wr\_adv) begin

if (tCVS > tAVS) begin

cre <= #(tCVS + tAVH) 1'b0;

adv\_n <= #(tCVS) 1'b1;

addr <= #(tCVS + tAVH) {32{1'bz}};

end else begin

cre <= #(tAVS + tAVH) 1'b0;

adv\_n <= #(tAVS) 1'b1;

addr <= #(tAVS + tAVH) {32{1'bz}};

end

end

#(tCW);

// save copy of configuration register (snoop addr bit 31 on cellular RAM 2.0 parts)

if (wr\_cre || ((GENERATION == CR20) && wr\_addr[ADDR\_BITS-1])) begin

set\_config\_reg\_copy(wr\_addr>>REG\_SEL, wr\_addr);

end

end

endtask

task async\_read;

input rd\_cre;

input [ADDR\_BITS-1:0] rd\_addr;

input [DQ\_BITS-1:0] rd\_data;

input [BY\_BITS:0] rd\_byte;

input rd\_adv;

begin

clk <= 1'b0;

adv\_n <= 1'b0;

cre <= 1'b0;

cre <= rd\_cre;

ce\_n <= 1'b0;

oe\_n <= 1'b1;

oe\_n <= #(tCO - tOE) 1'b0;

we\_n <= 1'b1;

if (GENERATION > CR10) begin

by\_n <= {BY\_BITS{1'b0}};

end else begin

by\_n <= rd\_byte;

end

addr <= rd\_addr;

if (rd\_adv) begin

if (tCVS > tAVS) begin

cre <= #(tCVS + tAVH) 1'b0;

adv\_n <= #(tCVS) 1'b1;

addr <= #(tCVS + tAVH) {32{1'bz}};

end else begin

cre <= #(tAVS + tAVH) 1'b0;

adv\_n <= #(tAVS) 1'b1;

addr <= #(tAVS + tAVH) {32{1'bz}};

end

end

#(tCO);

rd\_dm <= rd\_byte;

rd\_dq <= rd\_data;

rd\_comp <= #(tSP) 1'b1;

tm\_rd\_comp<= $realtime + tSP;

//keep data valid for a short time

#(tSP + tHD);

end

endtask

// one address cycle of a page mode read

task page\_read;

input [ADDR\_BITS-1 : 0] next\_addr;

input [DQ\_BITS-1:0] next\_data;

input [BY\_BITS:0] next\_byte;

begin

clk <= 1'b0;

adv\_n <= 1'b0;

cre <= 1'b0;

cre <= 1'b0;

ce\_n <= 1'b0;

oe\_n <= 1'b0;

we\_n <= 1'b1;

by\_n <= {BY\_BITS{1'b0}};

addr <= next\_addr;

if (addr[ADDR\_BITS-1:4] ^ next\_addr[ADDR\_BITS-1:4]) begin

#tAA;

end else begin

#tPC;

end

rd\_dm <= next\_byte;

rd\_dq <= next\_data;

rd\_comp <= #(tSP) 1'b1;

tm\_rd\_comp<= $realtime + tSP;

//keep data valid for a short time

#(tSP + tHD);

end

endtask

// controls how commands are terminated

task idle;

input [2:0] ctrl;

begin

// wait until any scheduled read compares are complete before ending the cycle

if (tm\_rd\_comp > $realtime) begin

//keep data valid for a short time

# (tm\_rd\_comp - $realtime + tHD);

end

case (ctrl)

0: begin

ce\_n <= 1'b1;

we\_n <= 1'b1;

by\_n <= {BY\_BITS{1'b1}};

oe\_n <= 1'b1;

adv\_n <= 1'b1;

end

1: we\_n <= 1'b1;

2: by\_n <= {BY\_BITS{1'b1}};

3: oe\_n <= 1'b1;

4: adv\_n <= 1'b1;

5: ce\_n <= 1'b1;

endcase

end

endtask

task sync\_write;

input wr\_cre;

input [ADDR\_BITS-1:0] wr\_addr;

input [DQ\_BITS-1:0] wr\_data;

input [BY\_BITS-1:0] wr\_byte;

integer i,w;

begin

clk\_pulse(2);

adv\_n <= #(0.5\*tclk - tSP) 1'b0;

adv\_n <= #(0.5\*tclk + tHD) 1'b1;

cre <= 1'bx;

cre <= #(0.5\*tclk - tSP) wr\_cre;

cre <= #(0.5\*tclk + tHD + tAVH) 1'bx;

ce\_n <= #(0.5\*tclk - tCSP) 1'b0;

oe\_n <= 1'b1;

we\_n <= #(tAS) 1'b0;

we\_n <= #(0.5\*tclk + tHD) 1'b1;

addr <= {32{1'bz}};

addr <= #(0.5\*tclk - tSP) wr\_addr;

addr <= #(0.5\*tclk + tHD + tAVH) {32{1'bz}};

#(1.5\*tclk);

i = 0;

while ((i\_wait !== 1'b0) && (i<WAIT\_LIMIT)) begin

#(0.5\*tclk);

// schedule first data word in burst in anticipation of WAIT going inactive

dq\_out <= #((0.5)\*tclk - tSP) wr\_data;

dq\_out <= #((0.5)\*tclk + tHD) {DQ\_BITS{1'bz}};

by\_n <= #((0.5)\*tclk - tSP) wr\_byte;

by\_n <= #((0.5)\*tclk + tHD) {BY\_BITS{1'b1}};

clk\_pulse(1);

#(0.5\*tclk);

i = i + 1;

end

if (i == WAIT\_LIMIT) begin

$display ("ENDING TEST: Wait not seen for %d clocks", WAIT\_LIMIT);

$stop();

end

#(0.5\*tclk);

// wait one more tclk if WAIT=1

if (bus\_configuration\_reg[8]) begin

dq\_out <= #((0.5)\*tclk - tSP) wr\_data;

dq\_out <= #((0.5)\*tclk + tHD) {DQ\_BITS{1'bz}};

by\_n <= #((0.5)\*tclk - tSP) wr\_byte;

by\_n <= #((0.5)\*tclk + tHD) {BY\_BITS{1'b1}};

clk\_pulse(1);

#(tclk);

end

clk <= 1'b0;

// save copy of configuration register (snoop addr bit 31 on cellular RAM 2.0 parts)

if (wr\_cre || ((GENERATION == CR20) && wr\_addr[ADDR\_BITS-1])) begin

set\_config\_reg\_copy(wr\_addr>>REG\_SEL, wr\_addr);

end

end

endtask

// one cycle of a sync write burst

task sync\_write\_burst;

input [DQ\_BITS-1:0] next\_data;

input [BY\_BITS:0] next\_byte;

begin

clk\_pulse(1);

adv\_n <= 1'b1;

cre <= 1'bx;

ce\_n <= 1'b0;

oe\_n <= 1'b1;

we\_n <= 1'b1;

by\_n <= #(0.5\*tclk - tSP) next\_byte;

by\_n <= #(0.5\*tclk + tHD) {BY\_BITS{1'b1}};

dq\_out <= #(0.5\*tclk - tSP) next\_data;

dq\_out <= #(0.5\*tclk + tHD) {DQ\_BITS{1'bz}};

#(tclk);

clk <= 1'b0;

end

endtask

task sync\_read;

input rd\_cre;

input [ADDR\_BITS-1:0] rd\_addr;

input [DQ\_BITS-1:0] rd\_data;

input [BY\_BITS-1:0] rd\_byte;

integer i;

begin

ce\_n <= 1'b0;

adv\_n <= 1'b0;

if (GENERATION > CR10) begin

by\_n <= {BY\_BITS{1'b0}};

end else begin

by\_n <= #((0.5)\*tclk - tSP) rd\_byte;

end

addr <= rd\_addr;

if (tAADV > ((bus\_configuration\_reg[13:11])+ 1.5)\*tclk) begin

#(tAADV-((bus\_configuration\_reg[13:11])+ 1.5)\*tclk);

end

clk\_pulse(2);

adv\_n <= #(0.5\*tclk + tHD) 1'b1;

cre <= 1'bx;

cre <= #(0.5\*tclk - tSP) rd\_cre;

cre <= #(0.5\*tclk + tHD + tAVH) 1'bx;

oe\_n <= 1'b1;

oe\_n <= #((0.5\*tclk) + tABA - tOE) 1'b0;

we\_n <= 1'b1;

addr <= #(0.5\*tclk + tHD + tAVH) {32{1'bz}};

#(1.5\*tclk);

i = 0;

while (((bus\_configuration\_reg[14] == 0) && (i\_wait !== 1'b0) && (i < WAIT\_LIMIT)) // variable latency = monitor wait

|| (bus\_configuration\_reg[14] && (i < (latency\_counter - 1)))) begin // fixed latency = use latency count from BCR

#(0.5\*tclk);

clk\_pulse(1);

#(0.5\*tclk);

i = i + 1;

end

if (i == WAIT\_LIMIT) begin

$display ("ENDING TEST: Wait not seen for %d clocks", WAIT\_LIMIT);

$stop();

end

rd\_dm <= #(tclk\*(bus\_configuration\_reg[8] || bus\_configuration\_reg[14])) rd\_byte;

rd\_dq <= #(tclk\*(bus\_configuration\_reg[8] || bus\_configuration\_reg[14])) rd\_data;

rd\_comp <= #(tclk\*(bus\_configuration\_reg[8] || bus\_configuration\_reg[14])) 1'b1;

tm\_rd\_comp<= $realtime + tclk\*(bus\_configuration\_reg[8] || bus\_configuration\_reg[14]);

#(0.5\*tclk);

clk <= 1'b0;

end

endtask

// one cycle of a sync read burst

task sync\_read\_burst;

input [DQ\_BITS-1:0] next\_data;

input [BY\_BITS:0] next\_byte;

reg [DQ\_BITS-1:0] bit\_mask;

begin

if ((bus\_configuration\_reg[8] == 0) && (bus\_configuration\_reg[14] == 0) && (next\_byte !== rd\_dm)) begin

$display ("%m at time %t: ERROR: Changing BY# during Sync Read is not supported with variable latency and wait configuration = 0", $time);

end

clk\_pulse(1);

adv\_n <= 1'b1;

cre <= 1'bx;

ce\_n <= 1'b0;

oe\_n <= 1'b0;

we\_n <= 1'b1;

if (GENERATION > CR10) begin

by\_n <= {BY\_BITS{1'b0}};

end else begin

by\_n <= #(0.5\*tclk - tSP) next\_byte;

end

#(0.5\*tclk);

rd\_dm <= #(tclk\*(bus\_configuration\_reg[8] || bus\_configuration\_reg[14])) next\_byte;

rd\_dq <= #(tclk\*(bus\_configuration\_reg[8] || bus\_configuration\_reg[14])) next\_data;

rd\_comp <= #(tclk\*(bus\_configuration\_reg[8] || bus\_configuration\_reg[14])) 1'b1;

tm\_rd\_comp<= $realtime + tclk\*(bus\_configuration\_reg[8] || bus\_configuration\_reg[14]);

#(0.5\*tclk);

clk <= 1'b0;

end

endtask

// nop, wait with clk low

task nop;

input wait\_time;

real wait\_time;

begin

clk <= 1'b0;

#(wait\_time);

end

endtask

always @(posedge rd\_comp) begin : data\_verify

integer i;

reg [DQ\_BITS-1:0] bit\_mask;

for (i=0; i<DQ\_BITS; i=i+1) begin

bit\_mask[i] = !rd\_dm[i/8];

end

// Verify the data word after output delay

if (((dq\_in & bit\_mask) ^ (rd\_dq & bit\_mask)) !== {DQ\_BITS{1'b0}}) begin

$display ("%m at time %t: ERROR: Read data miscompare: Expected = %h, Actual = %h, Mask = %h", $time, rd\_dq, dq\_in, bit\_mask);

//end else begin

// $display ("%m at time %t: INFO: Successful Read data compare: Expected = %h, Actual = %h, Mask = %h", $time, rd\_dq, dq\_in, bit\_mask);

end

rd\_comp <= 1'b0;

end

// End-of-test triggered in 'subtest.vh'

task test\_done;

begin

$display ("%m at time %t: INFO: Simulation is Complete", $time);

$stop(0);

end

endtask

// Test included from external file

`include "subtest.vh"

endmodule

Receive Engine Test Bench:

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

//

// Author: Victor Espinoza

// Email: victor.alfonso94@gmail.com

// Project #: Project 4 - Full UART Engine

// Course: CECS 460

//

// Create Date: 18:56:08 11/13/2015

//

// Module Name: receive\_engine\_tb

// File Name: receive\_engine\_tb.v

//

// Description: I verified that my Receive Engine was working correctly by using

// a simple test bench. In the Receive Engine test bench, I

// initialized my UART format to transfer at a baud rate of 300

// and have a format of 8O1. I then made sure that the receive

// engine correctly received the data of 0xAE. Since I extensively

// tested the Transmit Engine to make sure that I was able to

// successfully run at all of the different baud-rates and data

// formats (7N1, 7O1, 7E1, 8N1, 8O1m 8E1) for my project, I was

// convinced that the Receive Engine would yield the same results

// because the baud rate and format logic is almost identical

// between both engines. This is why I came to the conclusion that

// I did not need to test every possible baud-rate and data format

// combination for my Receive Engine. After I received the start bit

// from the receive data, I then waited for the bit time up to occur

// before I changed the Rx input value to the Receive Engine. This

// was so that I wasn't disturbing the Receive Engine while it was

// waiting for a bit time to begin collecting data. After a bit was

// shifted into the shift register, I then changed the Rx input in a

// way that would yield me receiving a byte of 0xAE. After all of the

// data bits were shifted into the shift register, I then loaded

// this data into a flop and sent the data to the PicoBlaze. As

// expected, the end result was that 0xAE was loaded into the flop

// and outputted to the PicoBlaze decoder (which selects what data

// is going to the In\_Port of the PicoBlaze) I also made sure that

// my Parity Error logic was correctly detecting a parity error by

// assigning the wrong parity to my byte of data. The 8O1 format

// should have an odd parity value of 0, but I gave the parity value

// a value of 1. As expected, The PARITY\_ERR status flag was set high

// and sent to the PicoBlaze decoder. I also made sure that all of my

// signals were changing correctly and that there were no surprises

// between the different states in my Receive Engine State Machine.

// This sums up what I did to verify the correctness of my Receive

// Engine. Note that I did not make a top level test bench for this

// project due to the sheer amount of transmits that I have to make

// for displaying the banner (it is a lot of characters!). Also, it

// is difficult to simulate the PicoBlaze receiving data because

// there is no terminal to display data through. This sums up how I

// verified the correctness of my Receive Engine.

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module receive\_engine\_tb;

//Inputs

reg clk;

reg rstb;

reg bit8;

reg parity\_en;

reg odd\_n\_even;

reg [3:0] baud\_val;

reg [1:0] READ;

reg Rx;

wire [2:0] status;

//Outputs

wire [7:0] data;

//Instantiate the Unit Under Test (UUT)

//receive\_engine(clk, rstb, bit8, parity\_en, odd\_n\_even, baud\_val, READ,

// Rx, status, data);

receive\_engine uut(

.clk(clk),

.rstb(rstb),

.bit8(bit8),

.parity\_en(parity\_en),

.odd\_n\_even(odd\_n\_even),

.baud\_val(baud\_val),

.READ(READ),

.Rx(Rx),

.status(status),

.data(data)

);

//vary the clk signal every 10ns to mimick a

//period of 20ns (which is the period of our boards)

always #10 clk = ~clk;

//always #20 tx\_Write = ~tx\_Write;

initial begin

//Initialize Inputs

clk = 0;

rstb = 0; //low active reset

//8O1 (460800 Baud) Transmitting 0xAE = 1010\_1110

bit8 = 1; //8 bits of data

parity\_en = 1; //parity enabled

odd\_n\_even = 1; //odd parity

baud\_val = 4'hA; //baud = 460800

Rx = 1'b0; //data to be transmitted

READ = 2'b00;

//Wait 100 ns for global reset to finish

#100 @(posedge clk) rstb = 1; // have reset become unactive.

READ = 2'b10;

#20 @(posedge clk)

READ = 2'b00;

//Receive 0xAE

wait (uut.btu == 1);

wait (uut.btu == 0);

Rx = 1'b1;

//d0

wait (uut.btu == 1);

wait (uut.btu == 0);

Rx = 1'b0;

//d1

wait (uut.btu == 1);

wait (uut.btu == 0);

Rx = 1'b1;

//d2

wait (uut.btu == 1);

wait (uut.btu == 0);

Rx = 1'b1;

//d3

wait (uut.btu == 1);

wait (uut.btu == 0);

Rx = 1'b1;

//d4

wait (uut.btu == 1);

wait (uut.btu == 0);

Rx = 1'b0;

//d5

wait (uut.btu == 1);

wait (uut.btu == 0);

Rx = 1'b1;

//d6

wait (uut.btu == 1);

wait (uut.btu == 0);

Rx = 1'b0;

//d7 / Parity / Stop

wait (uut.btu == 1);

wait (uut.btu == 0);

Rx = 1'b1;

wait (uut.done == 1); //wait until byte is done being received.

#200

$stop;

end

endmodule

Transmit Engine Test Bench:

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

//

// Author: Victor Espinoza

// Email: victor.alfonso94@gmail.com

// Project #: Project 3 - Transmit Engine plus PicoBlaze

// Course: CECS 460

//

// Create Date: 14:41:51 10/15/2015

//

// Module Name: transmit\_engine\_tb

// File Name: transmit\_engine\_tb.v

//

// Description: For this test bench I first initialized my Transmit Engine

// to be running at a 300 Baud Rate and at a 7N1 format. I then

// made sure that the correct value was getting loaded into my

// shift register and outputted the result of this comparison

// to the console. I then waited until the Done bit was set high,

// which signified that I was finished transmitting the 12 bits

// of data. I then loaded up the next byte of data, changed the

// baud rate to 1200, kept the 7N1 format, and repeated the

// process mentioned above. I made sure to transmit different

// combinations of data and to test out every format and

// baud rate available in my design. Once I verified that all

// of the data was being loaded and shifted out correctly at

// each of the different baud rates and data formats, I then

// concluded that my transmit engine was working correctly.

//

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module transmit\_engine\_tb;

//Inputs

reg clk;

reg rstb;

reg bit8;

reg parity\_en;

reg odd\_n\_even;

reg [3:0] baud\_val;

reg tx\_Write;

reg [7:0] in\_data;

//Outputs

wire tx; //transferLimitReached;

wire TxRdy;

//Instantiate the Unit Under Test (UUT)

//module transmit\_engine(clk, rstb, bit8, parity\_en, odd\_n\_even, baud\_val, txWrite,

//inData, tx, TxRdy);

transmit\_engine uut(

.clk(clk),

.rstb(rstb),

.bit8(bit8),

.parity\_en(parity\_en),

.odd\_n\_even(odd\_n\_even),

.baud\_val(baud\_val),

.txWrite(tx\_Write),

.inData(in\_data),

.tx(tx),

.TxRdy(TxRdy)

);

//vary the clk signal every 10ns to mimick a

//period of 20ns (which is the period of our boards)

always #10 clk = ~clk;

//always #20 tx\_Write = ~tx\_Write;

initial begin

//Initialize Inputs

clk = 0;

rstb = 0; //low active reset

//7N1 (300 Baud) Transmitting 0x65 = 110\_0101

bit8 = 0; //7 bits of data

parity\_en = 0; //parity disabled

odd\_n\_even = 0; //no parity

baud\_val = 4'h0; //baud = 300

in\_data = 8'h65; //data to be transmitted

//Wait 100 ns for global reset to finish

#100 @(posedge clk) rstb = 1; // have reset become unactive.

tx\_Write = 1; //assert tx\_Write after reset.

#20 @(posedge clk) tx\_Write = 0;

@(posedge clk) if(uut.write1Delay == 1)begin

#20; //wait for next clock cycle (when data is updated)

if (uut.sreg\_data != 12'hf95) //7N1 tx -> 0x65 = f95

$display("Incorrect Data! Expected: 0xf95 , Actual: 0x%h",

uut.sreg\_data[11:0]);

else

$display("Correct Data! Expected: 0xf95 , Actual: 0x%h",

uut.sreg\_data[11:0]);

end

wait (uut.Done == 1); //wait until byte is done being transmitted.

wait (uut.TxRdy == 1); //wait until transmit engine is ready

//to receive another byte.

wait (uut.Done == 0); //wait until byte is done being transmitted.

//7N1 (1200 Baud) Transmitting 0x54 = 101\_0100

bit8 = 0; //7 bits of data

parity\_en = 0; //parity disabled

odd\_n\_even = 1; //no parity

baud\_val = 4'h1; //baud = 1200

in\_data = 8'h54; //data to be transmitted

tx\_Write = 1; //assert tx\_Write

#20 @(posedge clk) tx\_Write = 0; //deassert tx\_Write

@(posedge clk) if(uut.write1Delay == 1)begin

#20; //wait for next clock cycle (when data is updated)

if (uut.sreg\_data != 12'hf51) //7N1 tx -> 0x54 = f51

$display("Incorrect Data! Expected: 0xf51 , Actual: 0x%h",

uut.sreg\_data[11:0]);

else

$display("Correct Data! Expected: 0xf51 , Actual: 0x%h",

uut.sreg\_data[11:0]);

end

wait (uut.Done == 1); //wait until byte is done being transmitted.

wait (uut.TxRdy == 1); //wait until transmit engine is ready

//to receive another byte.

wait (uut.Done == 0); //wait until byte is done being transmitted.

//7E1 (2400 Baud) Transmitting 0x72 = 111\_0010

bit8 = 0; //7 bits of data

parity\_en = 1; //parity enabled

odd\_n\_even = 0; //even parity

tx\_Write = 1; //assert tx\_Write

baud\_val = 4'h2; //baud = 2400

in\_data = 8'h72; //data to be transmitted

#20 @(posedge clk) tx\_Write = 0; //deassert tx\_Write

@(posedge clk) if(uut.write1Delay == 1)begin

#20; //wait for next clock cycle (when data is updated)

if (uut.sreg\_data != 12'hdc9) //7E1 tx -> 0x72 = dc9

$display("Incorrect Data! Expected: 0xdc9 , Actual: 0x%h",

uut.sreg\_data[11:0]);

else

$display("Correct Data! Expected: 0xdc9 , Actual: 0x%h",

uut.sreg\_data[11:0]);

end

wait (uut.Done == 1); //wait until byte is done being transmitted.

wait (uut.TxRdy == 1); //wait until transmit engine is ready

//to receive another byte.

wait (uut.Done == 0); //wait until byte is done being transmitted.

//7O1 (4800 Baud) Transmitting 0x4F = 100\_1111

bit8 = 0; //7 bits of data

parity\_en = 0; //parity disabled

odd\_n\_even = 1; //no parity

tx\_Write = 1; //assert tx\_Write

baud\_val = 4'h3; //baud = 4800

in\_data = 8'h4F; //data to be transmitted

#20 @(posedge clk) tx\_Write = 0; //deassert tx\_Write

@(posedge clk) if(uut.write1Delay == 1)begin

#20; //wait for next clock cycle (when data is updated)

if (uut.sreg\_data != 12'hf3d) //7O1 tx -> 0x4f = f3d

$display("Incorrect Data! Expected: 0xf3d , Actual: 0x%h",

uut.sreg\_data[11:0]);

else

$display("Correct Data! Expected: 0xf3d , Actual: 0x%h",

uut.sreg\_data[11:0]);

end

wait (uut.Done == 1); //wait until byte is done being transmitted.

wait (uut.TxRdy == 1); //wait until transmit engine is ready

//to receive another byte.

wait (uut.Done == 0);

//8N1 (9600 Baud) Transmitting 0x4F = 0100\_1111

bit8 = 1; //8 bits of data

parity\_en = 0; //parity enabled

odd\_n\_even = 0; //no parity

tx\_Write = 1; //assert tx\_Write

baud\_val = 4'h4; //baud = 9600

in\_data = 8'h4F; //data to be transmitted

#20 @(posedge clk) tx\_Write = 0; //deassert tx\_Write

@(posedge clk) if(uut.write1Delay == 1)begin

#20; //wait for next clock cycle (when data is updated)

if (uut.sreg\_data != 12'hd3d) //8N1 tx -> 0x4f = d3d

$display("Incorrect Data! Expected: 0xd3d , Actual: 0x%h",

uut.sreg\_data[11:0]);

else

$display("Correct Data! Expected: 0xd3d , Actual: 0x%h",

uut.sreg\_data[11:0]);

end

wait (uut.Done == 1); //wait until byte is done being transmitted.

wait (uut.TxRdy == 1); //wait until transmit engine is ready

//to receive another byte.

wait (uut.Done == 0);

//8N1 (19200 Baud) Transmitting 0xAE = 1010\_1110

bit8 = 1; //8 bits of data

parity\_en = 0; //parity enabled

odd\_n\_even = 1; //no parity

tx\_Write = 1; //assert tx\_Write

baud\_val = 4'h5; //baud = 19200

in\_data = 8'hAE; //data to be transmitted

#20 @(posedge clk) tx\_Write = 0; //deassert tx\_Write

@(posedge clk) if(uut.write1Delay == 1)begin

#20; //wait for next clock cycle (when data is updated)

if (uut.sreg\_data != 12'heb9) //8N1 tx -> 0xAE = eb9

$display("Incorrect Data! Expected: 0xeb9 , Actual: 0x%h",

uut.sreg\_data[11:0]);

else

$display("Correct Data! Expected: 0xeb9 , Actual: 0x%h",

uut.sreg\_data[11:0]);

end

wait (uut.Done == 1); //wait until byte is done being transmitted.

wait (uut.TxRdy == 1); //wait until transmit engine is ready

//to receive another byte.

wait (uut.Done == 0);

//8E1 (38400 Baud) Transmitting 0xBD = 1011\_1101

bit8 = 1; //8 bits of data

parity\_en = 1; //parity enabled

odd\_n\_even = 0; //even parity

tx\_Write = 1; //assert tx\_Write

baud\_val = 4'h6; //baud = 38400

in\_data = 8'hBD; //data to be transmitted

#20 @(posedge clk) tx\_Write = 0; //deassert tx\_Write

@(posedge clk) if(uut.write1Delay == 1)begin

#20; //wait for next clock cycle (when data is updated)

if (uut.sreg\_data != 12'haf5) //8E1 tx -> 0xBD = af5

$display("Incorrect Data! Expected: 0xaf5 , Actual: 0x%h",

uut.sreg\_data[11:0]);

else

$display("Correct Data! Expected: 0xaf5 , Actual: 0x%h",

uut.sreg\_data[11:0]);

end

wait (uut.Done == 1); //wait until byte is done being transmitted.

wait (uut.TxRdy == 1); //wait until transmit engine is ready

//to receive another byte.

wait (uut.Done == 0);

//8O1 (57600 Baud) Transmitting 0x4F = 0000\_1000

bit8 = 1; //8 bits of data

parity\_en = 1; //parity enabled

odd\_n\_even = 1; //odd parity

tx\_Write = 1; //assert tx\_Write

baud\_val = 4'h7; //baud = 57600

in\_data = 8'h08; //data to be transmitted

#20 @(posedge clk) tx\_Write = 0; //deassert tx\_Write

@(posedge clk) if(uut.write1Delay == 1)begin

#20; //wait for next clock cycle (when data is updated)

if (uut.sreg\_data != 12'h821) //8O1 tx -> 0x08 = 821

$display("Incorrect Data! Expected: 0x821 , Actual: 0x%h",

uut.sreg\_data[11:0]);

else

$display("Correct Data! Expected: 0x821 , Actual: 0x%h",

uut.sreg\_data[11:0]);

end

wait (uut.Done == 1); //wait until byte is done being transmitted.

wait (uut.TxRdy == 1); //wait until transmit engine is ready

//to receive another byte.

wait (uut.Done == 0);

//8O1 (115200 Baud) Transmitting 0x4F = 0100\_1111

bit8 = 1; //8 bits of data

parity\_en = 1; //parity enabled

odd\_n\_even = 1; //odd parity

tx\_Write = 1; //assert tx\_Write

baud\_val = 4'h8; //baud = 115200

in\_data = 8'h4F; //data to be transmitted

#20 @(posedge clk) tx\_Write = 0; //deassert tx\_Write

@(posedge clk) if(uut.write1Delay == 1)begin

#20; //wait for next clock cycle (when data is updated)

if (uut.sreg\_data != 12'h93d) //8O1 tx -> 0x4F = 93d

$display("Incorrect Data! Expected: 0x93d , Actual: 0x%h",

uut.sreg\_data[11:0]);

else

$display("Correct Data! Expected: 0x93d , Actual: 0x%h",

uut.sreg\_data[11:0]);

end

wait (uut.Done == 1); //wait until byte is done being transmitted.

wait (uut.TxRdy == 1); //wait until transmit engine is ready

//to receive another byte.

wait (uut.Done == 0);

//8O1 (230400 Baud) Transmitting 0x00 = 0000\_0000

bit8 = 1; //8 bits of data

parity\_en = 1; //parity enabled

odd\_n\_even = 1; //odd parity

tx\_Write = 1; //assert tx\_Write

baud\_val = 4'h9; //baud = 230400

in\_data = 8'h00; //data to be transmitted

#20 @(posedge clk) tx\_Write = 0; //deassert tx\_Write

@(posedge clk) if(uut.write1Delay == 1)begin

#20; //wait for next clock cycle (when data is updated)

if (uut.sreg\_data != 12'hc01) //8O1 tx -> 0x00 = c01

$display("Incorrect Data! Expected: 0xc01 , Actual: 0x%h",

uut.sreg\_data[11:0]);

else

$display("Correct Data! Expected: 0xc01 , Actual: 0x%h",

uut.sreg\_data[11:0]);

end

wait (uut.Done == 1); //wait until byte is done being transmitted.

wait (uut.TxRdy == 1); //wait until transmit engine is ready

//to receive another byte.

wait (uut.Done == 0);

//8O1 (460800 Baud) Transmitting 0x55 = 0101\_0101

bit8 = 1; //8 bits of data

parity\_en = 1; //parity enabled

odd\_n\_even = 1; //odd parity

tx\_Write = 1; //assert tx\_Write

baud\_val = 4'hA; //baud = 460800

in\_data = 8'h55; //data to be transmitted

#20 @(posedge clk) tx\_Write = 0; //deassert tx\_Write

@(posedge clk) if(uut.write1Delay == 1)begin

#20; //wait for next clock cycle (when data is updated)

if (uut.sreg\_data != 12'hd55) //8O1 tx -> 0x55 = d55

$display("Incorrect Data! Expected: 0xd55 , Actual: 0x%h",

uut.sreg\_data[11:0]);

else

$display("Correct Data! Expected: 0xd55 , Actual: 0x%h",

uut.sreg\_data[11:0]);

end

wait (uut.Done == 1); //wait until byte is done being transmitted.

wait (uut.TxRdy == 1); //wait until transmit engine is ready

//to receive another byte.

wait (uut.Done == 0);

//8O1 (921600 Baud) Transmitting 0x4F = 0010\_0000

bit8 = 1; //8 bits of data

parity\_en = 1; //parity enabled

odd\_n\_even = 1; //odd parity

tx\_Write = 1; //assert tx\_Write

baud\_val = 4'hB; //baud = 921600

in\_data = 8'h20; //data to be transmitted

#20 @(posedge clk) tx\_Write = 0; //deassert tx\_Write

@(posedge clk) if(uut.write1Delay == 1)begin

#20; //wait for next clock cycle (when data is updated)

if (uut.sreg\_data != 12'h881) //8O1 tx -> 0x20 = 881

$display("Incorrect Data! Expected: 0x881 , Actual: 0x%h",

uut.sreg\_data[11:0]);

else

$display("Correct Data! Expected: 0x881 , Actual: 0x%h",

uut.sreg\_data[11:0]);

end

wait (uut.Done == 1); //wait until byte is done being transmitted.

wait (uut.TxRdy == 1); //wait until transmit engine is ready

//to receive another byte.

wait (uut.Done == 0);

$stop;

end

endmodule